DESIGN AND DEMONSTRATION OF EMBEDDED INDUCTORS FOR HIGH-VOLTAGE INTEGRATED VOLTAGE REGULATORS.

A Dissertation
Presented to
The Academic Faculty

By

Claudio Alvarez Barros

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Engineering
Department of Electrical and Computer Engineering

Georgia Institute of Technology

August 2021

DESIGN AND DEMONSTRATION OF EMBEDDED INDUCTORS FOR HIGH-VOLTAGE INTEGRATED VOLTAGE REGULATORS.

Thesis committee:

Dr. Madhavan Swaminathan
School of Electrical and Computer Engineering, joint appointment with School of Material Science and Engineering/Professor; Director, 3D Systems Packaging Research Center (PRC)
Georgia Institute of Technology

Dr. Arijit Raychowdhury
School of Electrical and Computer Engineering/Professor
Georgia Institute of Technology

Dr. Saibal Mukhopadhyay
School of Electrical and Computer Engineering/Professor
Georgia Institute of Technology

Dr. Mark Losego
School of Material Science and Engineering/Professor
Georgia Institute of Technology

Dr. Kaladhar Radhakrishnan
Technology Development Group/Senior Principal Engineer
Intel Corporation.

Date approved: July 12, 2021

To my wife Karen, and my sons Daniel and Matias.

ACKNOWLEDGMENTS

First and foremost, I want to thank my advisor prof. Madhavan Swaminathan who always supported and guided me through my research work. He allowed me to be part of the Center for Co-design of Chip, Package and System (C3PS), the Georgia Tech Packaging Research Center (GT-PRC), and the SRC JUMP program. His vision on electronic packaging and passive components helped me to focus my work and obtain valuable results for the academia and industry. I would also like to thank the PRC professors, researchers, and staff, who shared with me their acknowledgment, support, and help, including Dr. Bidyut Bhattacharyya, Dr. Jack Moon, Dr. Vanessa Smet, Dr. Fuhan Liu, Dr. Mohan Kathaperuma, Dr. Himani Sharma, Chris White, Lila Dahal, Carol Mills, and Shari Tavares. I would also like to thank professors Arijit Raychowdhury, Saibal Mukhopadhyay, Mark Losego, and Dr. Kaladhar Radhakrishnan for being part of my thesis defense committee and provide me valuable feedback.

I want to, especially, thank Srinidhi for sharing her expertise on materials and fabrication processes, and for taking charge of the fabrication of the first version of the inductors presented in this work. In addition, his knowledge of manufacturing matters guided my design so that it could be manufactured. I also want to thank Prahalad Murali for taken over the inductor fabrication after Shrinidi graduate. Both of them, with their infinite patience, helped me to fabricate over 100 inductors until we got them working.

Being part of the C3PS and PRC group let me share laughs and acknowledge with many people, including Osama Waqar, Mutee Ur Rehman, Nahid Aslani, Sridhar Sivapurapu, Hakki Torun, Kai-Qi Huan, Majid Ahadi, Seunghyup Han, Siddharth Ravichandran, and Atom Watanabe.

I can't possibly express how grateful I am to my wife who took the most demanding task of taking care of our two sons, Daniel (4yr) and Matias (2yr), while I was in the lab or classes. Without her support, it would have been impossible for me to finish my Ph.D. I

want to thank my parents and my brother who have helped and supported me since always, with education, entertainment, love, happiness, and visiting us to help us with our kids.

This work was supported in part by ASCENT, one of six centers in JUMP, a Semiconductor Research Corporation (SRC) program sponsored by DARPA. Assigned SRC Task numbers 2776.032 and 2776.033.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

System on Chips (SoC) and processors (CPU), for high-performance computing (HPC) applications, require to run at very high-speed and high-power consumption levels. High bandwidth and high-performance power supplies are required to make these applications possible. On-board or printed circuit board (PCB) power supplies cannot meet these tight requirements. However, power supplies built in the same SoC package, called Integrated Voltage Regulators or IVRs, can reduce the power distribution network (PDN) impedance and increase the regulation bandwidth, as they operate at several MHz. Typical SoCs are powered with 1.7 V, but with power consumption rising over 100 W the input current starts to go over 65 A which becomes a problem.

The trend for next-generation HPC platforms is to supply the SoC directly with 12 V or 48 V. At these input voltages, the IVR is restricted to work around 2 MHz for high switching efficiency, due to the high MOSFET losses. However, at this frequency, the required inductance can be over 400 nH while the DC resistance must be below 20 mΩ. In addition, single stage 48 V to 1 V or 12 V to 1 V conversion ratios present new challenges that are not seen in low voltage converters such as 3.3 V or 1.7 V to 1 V. New metrics for magnetic materials and inductor technologies are required to describes their efficiency under different duty cycle conditions. The efficiency conditions for the inductor operation must be matched by the power stage topology, leading to a co-design between the power inductor (material science and electromagnetism) and the power stage topology (power electronics).

The objectives of this research are the design, modeling, fabrication, and characterization of embedded inductors for high voltage IVRs. The result of this study is a set of design rules and a design framework that allows evaluating the performance of an inductor with a new metric called Effective AC resistance per unit inductance or R_{acx}. With this metric, we present both the limitations of the current technology and the roadmap of magnetic

materials that can allow fabricating high-performance embedded inductors.

This work takes a look into different power stage topologies that aims to solve the low efficiency at high voltage and high frequency. It also analyzes the power loss breakdown to identify the main source of losses. Different inductor properties are considered to be able to design a new inductor for this particular application. A new fabrication process is developed, where slots are drilled in a magnetic substrate and filled with a dielectric. Vias are then drilled in the dielectric to form vias-in-slots which finally form the inductor windings. Seven different inductor designs were fabricated using 6 different magnetic materials (in the form of metal-polymer composites magnetic sheets), three with flake fillers, and three with spherical fillers. In total, 42 inductors are characterized, which allows comparing the performance of a broad range of inductors, from a few nH to over 500 nH, with DC resistance between 10 mΩ to 40 mΩ, saturation current from less than 100 mA to over 5 A, and over a frequency span from 100 kHz to 1 GHz.

This comprehensive set of comparisons include the small-signal inductance and resistance spectra with and without DC bias current, and the large-signal inductance and losses. Using the R_{acx} metric, this work shows that it is possible to evaluate new magnetic materials using a simple discrete toroidal inductor (that takes one day to fabricate) and predict with it the performance of more complex embedded inductors (that can take several months of work). This thesis concludes with the magnetic material research roadmap, where it is presented the required magnetic properties that, when using in combination with the technologies developed in this work, can allow a single-stage 12 V to 1 V and 48 V to 1 V integrated voltage regulators.

CHAPTER 1

INTRODUCTION AND LITERATURE REVIEW

The increased demand in computational capacity and size miniaturization, for emerging electronic devices, is setting new levels of efficiency and thermal constraints on power delivery systems. Since the power consumption has increased, the trend is to supply high-performance computing (HPC) platforms with 48 V. Multi-stage converters had been used for this purpose, but they suffer from high losses due to many components. In this research, embedded inductors for single stage 48 V to 1 V or 12 V to 1 V Integrated Voltage Regulators (IVRs) are explored to increase both performance and efficiency. This is motivated by Power Integrity (PI), Power Delivery Network (PDN), and power conversion efficiency problems. However, high conversion ratio converters present new challenges for power stage topologies and inductor technologies.

1.1 Motivation

System on chip (SoC) and processors (CPU) in servers and data centers require several down conversion stages to convert the grid voltage, ranging from 85 V to 265 V AC, to 1 V DC [1]. These down conversion stages include power factor correction that converts the grid voltage to 400 V_{DC}, a buck converter from 400 V_{DC} to 48 V, and several stages to convert from 48 V to 1 V, as shown in Figure 1.1.

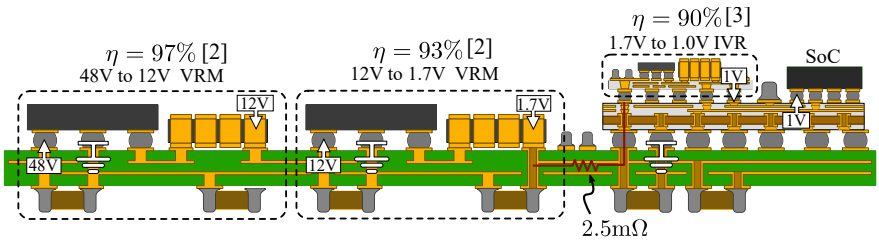


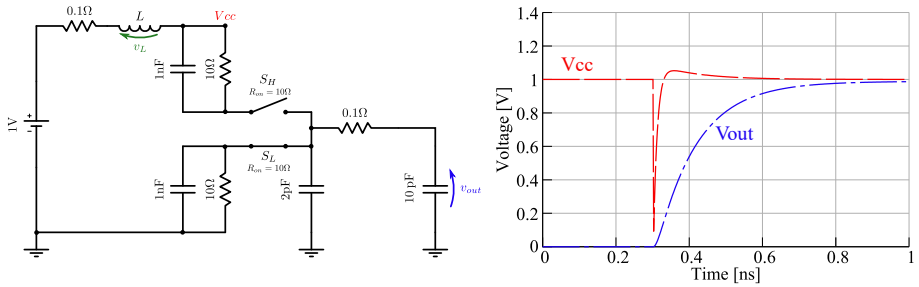
Figure 1.1: Multi-stage power delivery network for voltage down conversion from 48 V to 1 V.

In [2], two buck converters are presented using Gallium-Nitride (GaN) MOSFET with reported efficiencies of 97% for 48 V to 12 V and 93% for 12 V to 1.7 V. In [3] an IVR is presented for 1.7 V to 1 V conversion with a 90% efficiency. Assuming an SoC power consumption of 90 W and a power delivery network (PDN) DC resistance of 2.5 mΩ (between the last on-board voltage regulator and the IVR [4]), this multi-stage down-conversion system shows a combined efficiency of 75%. This means that, from the 120 W provided by the 48 V power supply, 30 W are lost. Since the IVR shown in [3] has a peak efficiency of 90%, the power delivered to the SoC package is 100 W or 58.8 A at 1.7 V. With this amount of current, the routing losses over the 2.5 mΩ resistance of the interconnection between the package and the board is 8.64 W, which is almost half of the losses between the 48 V power supply and IVR input. If instead, an IVR with 5 V or 12 V input is used, the routing losses can be reduced to 1 W and 0.174 W, respectively. The increase of regulation bandwidth and reduction of routing losses are the main motivation for high-voltage IVRs.

From the load point of view, in digital systems the signals are generated using digital Input-Output (IO) buffers to produce either a logic 0 or 1, which corresponds to an output voltage zero or non-zero, respectively. But due to RLC parasitic in the signal path, the signal levels do not change instantaneously. The time taken to change the state is called rise-time t_r or fall-time t_f. The t_r and t_f characteristics determine the maximum data rate of the channel. However, they are also a function of the power supply voltage, and additional jitter is introduced when the supply voltage changes considerably.

The stability of the supply voltage depends on its response time or bandwidth, the PDN impedance, the IO buffer current consumption, and the IO operating frequency. Figure 1.2(a) shows a simple IO buffer model connected to a power supply with parasitic inductance and resistance in between. Figure 1.2(b) shows the V_{CC} voltage drop when v_{out} change from 0 to V_{CC} when $L = 1$ nH. To prevent this drop several capacitors must be placed between the power source and the load. Figure 1.3(a) shows a more complete PDN network with the board, package, and IC decoupling capacitors. Figure 1.3(b) shows how

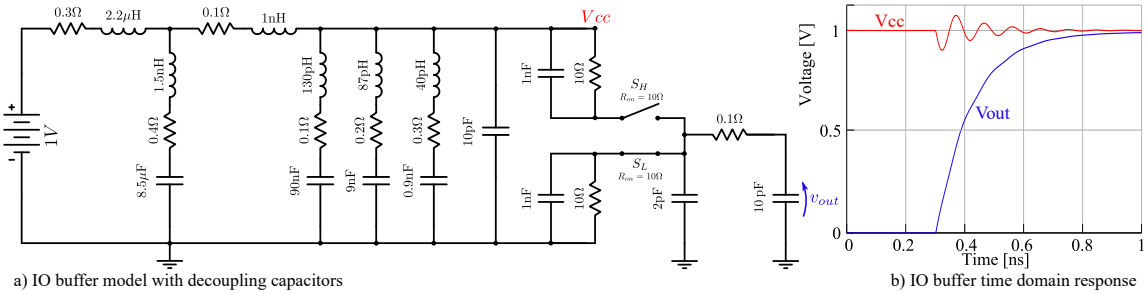
the voltage drop is significantly reduced.



a) IO buffer model

b) IO buffer time domain response

Figure 1.2: Digital IO buffer model and time domain response with parasitic inductance $L = 1$ nH.



a) IO buffer model with decoupling capacitors

b) IO buffer time domain response

Figure 1.3: Digital IO buffer model with decoupling capacitors and time domain response.

There are two ways to improve the PDN frequency response: i) place the power source as close as possible to the load to reduced the PDN impedance, and ii) increase the power source bandwidth to reduce its output impedance. These two solutions can be addressed by replacing the multi-stage system with a single-stage voltage regulator, which will also reduce the routing losses. When this voltage regulator is part of the same SoC package it is called an Integrated Voltage Regulator or IVR. Figure 1.4(a) and Figure 1.4(b) show scenarios for 12 V to 1 V and 48 V to 1 V IVRs. IVRs with switching frequencies over 10 MHz allow the usage of smaller passives components and can improve the system dynamics since the converter has higher bandwidth allowing for faster transient response [5].

There are several types of IVRs depending on the integration level, as shown in Figure 1.5. As the figure shows, the highest integration density is achieved when embedded inductors are used. In this thesis, we work on the concept of package IVRs with embedded inductors. The use of IVRs can improve the overall system efficiency and, as they

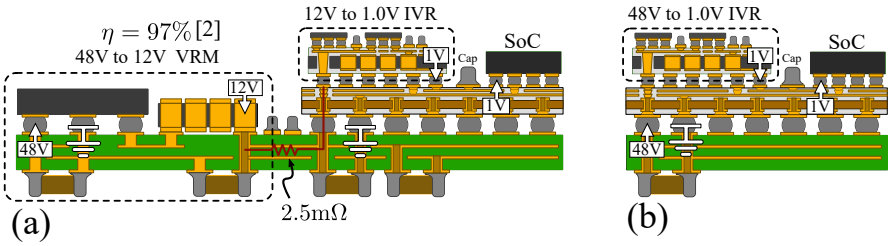


Figure 1.4: Different power distribution networks. (a) Two-stage 48V-12V with 12V-1.0V IVR down converter, (b) single-stage 48V-1.0V IVR.

use switching frequencies of several MHz, the converter has higher bandwidth allowing a faster transient response [5]. Also, due to its proximity to the load, they need less decoupling capacitance. However, for IVRs it is challenging to fabricate ultra-high-performance embedded inductors, and because of the high input voltage of 48V or 12V the switching losses in the MOSFET are very high which limits the maximum frequency of operation.

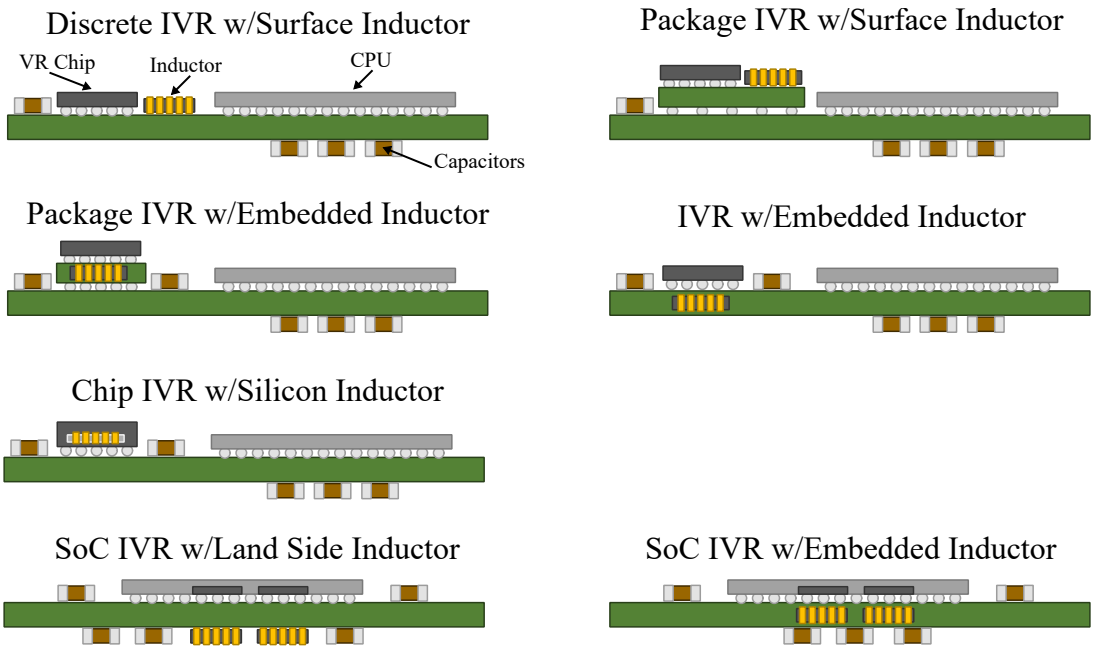


Figure 1.5: Types of IVR according to its integration level.

The amount of inductance a buck converter requires is calculated based on the conversion ratio, frequency, and maximum current ripple. In IVRs, the inductors are space constrained and only a small inductance can be embedded in the package. To solve this

problem, IVRs need to work at very high switching frequencies typically over 10 MHz. At these frequencies, the required inductance is in the order of 10's of nH, but with the drawback that only low conversion ratios of 5 V (or lower) to 1V are possible. Typical inductors for low conversion ratio have very high DC resistance with DC resistance to inductance ratio greater than 1 mΩ/nH.

Since high conversion ratio converters of 48V to 1V and 12V to 1V are limited to frequencies of 5 MHz or less, the required amount of inductance can be between 150 nH to 450 nH while keeping a DC resistance less than 20 mΩ. These inductors require a DC resistance to inductance ratio less than 0.1 mΩ/nH which can not be achieved with current IVR inductor technology.

1.2 Inductors

Every time an electric current flows through a conductor, a magnetic field is produced. This magnetic field will react to any changes in the current to oppose its change. The work done to prevent this change is done using energy stored in this magnetic field. A passive component that uses this principle on purpose to store energy is called an inductor, and its capacity to store energy is called inductance and is measured in Henry (H).

When a magnetic flux field changes, an opposing electromotive force (EMF) is produced. The proportion of this EMF to the change in electric current producing the field corresponds to the inductance, and is given by the next relation of Faraday's law,

$$v(t) = -\frac{d\phi}{dt} = L\frac{di}{dt} \tag{1.1}$$

and therefore, the inductance is given by,

$$L = -\frac{\phi(i)}{i} \tag{1.2}$$

As was mentioned, the inductance is also a measure of how much energy is stored. This

magnetic energy is given by,

$$U = \int_0^I L(i) i di \tag{1.3}$$

and, if the inductance L can be considered constant over the integration limits, then the stored energy is $U = 1/2LI^2$. The more inductance an inductor has, the more energy is stored in a given volume.

The inductance of an inductor can be increased when, instead of air, the inductor is built with magnetic materials. Magnetic materials are characterized by a permeability greater than the permeability of free space μ_0. Using a magnetic substrate, several inductor structures are possible, as shown in Figure 1.6. They can be classified into open-magnetic-path and closed-magnetic-path. When the magnetic flux lines pass through the air it is said to be an open magnetic path inductor. When the magnetic flux is always contained in magnetic material it is said to be a close magnetic path inductor.

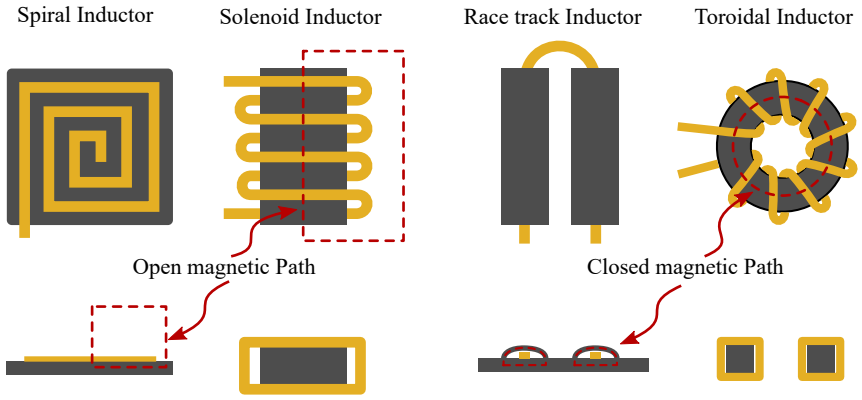


Figure 1.6: Typical inductor structures.

The inductance can be calculated analytically when ideal structures are considered, however, only a simplified analysis is introduced here. The magnetic flux $\phi(t)$ can be calculated from Ampere's law $\oint \vec{H} dl = i$ as follow (assuming $\vec{H}$ is constant along the

integration path),

$$\oint \vec{H} dl = Hl = Ni(t) \Rightarrow H = \frac{Ni(t)}{l}$$
$$\phi(t) = \mu_0 \mu_r \int_S \vec{H} dA = \mu_0 \mu_r N i(t) \frac{A}{l}$$

where N is the number of enclosed turns, and l is the magnetic path length (only along the magnetic material). The surface integral is over the cross-section of the inductor. With this result, we can approximate the inductance value,

$$L \approx \mu_u \mu_e \frac{N^2 A}{l} \tag{1.4}$$

where μ_e is the effective relative permeability, which is smaller than the material relative permeability μ_r due to demagnetization effects, shape anisotropy, partially filling with material, and air inductance contribution. The relation A/l (cross section area over magnetic path length) means that the inductance can be kept the same when an inductor is made smaller provided that this ratio remains the same, but there is always a limit on how much energy can be stored in a reduced space. The current at which no more energy can be stored, or the inductance starts to suddenly drop, is called saturation current I_{sat}. In this work, only solenoids and toroids are studied.

Ideal inductors at room temperature don't exist yet. This means the inductor will not only store and transfer energy but also will lose some amount of it in the process. There exist several mechanisms of losses in an inductor, and the most important are: i) core losses due to magnetic hysteresis, ii) eddy current losses in the magnetic material, and iii) copper losses due to DC resistance and skin and proximity effect. In addition, all these losses increase when non-sinusoidal excitation are applied, wherein such case, all the inductor current harmonics will create additional losses.

The hysteresis losses can be derived from the definition of energy loss in a device, per

switching cycle,

$$U = \int_0^T v_L(t) i_L(t)\, dt \tag{1.5}$$

Replacing the voltage and current by its equivalent form from Faraday's law and Ampere's law [6], we obtain,

$$U = \int_0^T \left(NA\frac{dB}{dt} \right) \left(\frac{Hl}{N} \right) dt = Al \int H\, dB \tag{1.6}$$

where N is the number of turns, A is the cross section area, and l is the mean magnetic path length. Then, the power loss, due to hysteresis, is found by multiplying U by the switching frequency,

$$P_H = Al \int H\, dB \cdot f_s \tag{1.7}$$

The eddy current losses are the result of the conductive nature of most magnetic materials. From Faraday's law, every changing magnetic field will produce an electromotive force (EMF),

$$EMF = -\frac{d\phi_B(t)}{dt} \tag{1.8}$$

Due to the conductivity of the material, this electromotive force will induce a current that will dissipate energy in form of heat. Materials with low conductivity are then preferred to reduce these losses.

Since the inductors are built with copper coils, the copper resistance will also dissipate energy. At higher frequency, eddy currents with the opposite direction are induced inside the conductor increasing its resistance. The skin depth is the distance from the conductor surface that is effectively used to conduct current, and is given by,

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \tag{1.9}$$

where ρ is the material resistivity, μ is the material permeability, and f is the current fre-

quency. Then the AC resistance of copper is,

$$R_{AC} = \frac{r}{\delta} R_{DC} \tag{1.10}$$

where r is the conductor radius and R_{DC} is the DC resistance.

Typically, the amount of inductance required in a buck converter is driven by a maximum inductor current ripple Δi_L, a given output voltage V, and switching duty cycle D and period T_s,

$$L = \frac{V}{2\Delta i_L}(1 - D)T_s \tag{1.11}$$

However, for high-performance voltage regulators, the design must be based on the inductor efficiency with the maximum current ripple, maximum frequency, and minimum duty cycle as a constraint. In [7, 8] a comparison of inductor cores loss calculation methods are presented, including the Steinmetz Equation (SE), Modified Stainmetz Equation (MSE), and Generalized Stainmetz Equation (GSE). In these methods, the losses are estimated by the next formulas where several coefficients must be experimentally obtained.

$$P_{c|SE} = k \cdot f^{\alpha} \cdot B_m^{\beta} \tag{1.12}$$

$$P_{c|MSE} = (k \cdot f_{eq}^{\alpha-1} \cdot B_m^{\beta})) \cdot f \quad , \quad f_{eq} = \frac{2}{\Delta B^2 \pi^2} \int_0^T \left(\frac{dB}{dt}\right)^2 dt \tag{1.13}$$

$$P_{c,GSE} = \frac{k_1}{T} \int_0^T \left|\frac{dB}{dt}\right|^{\alpha} |B(t)|^{\beta-\alpha} dt \quad , \quad k_1 = \frac{k}{2^{\beta-\alpha}(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} d\theta} \tag{1.14}$$

In [8], these methods are compared for non-sinusoidal excitation in switched-mode power supplies at 10 kHz. It shows how the core losses increase when the switching duty cycle moves away from 50%. This increase of losses is the result of the inductor current harmonics. As shown in [8] through measurements, the SE model cannot predict the loss variation as a function of the duty cycle, while the MSE and GSE methods have an error of +10% at 0.5 duty cycle and -25% at 0.1 duty cycle. Since in high voltage IVRs the duty cycles can be around 0.2 or lower, an accurate method to calculate the losses is required.

In [9], it is shown that the magnetic hysteresis losses are static, and the wider hysteresis at higher frequencies is due to an apparent increase in the magnetic coercivity, where the increment in coercivity is due to eddy current losses, not a change in the hysteresis curve. In [9] it is also shown that when the magnetic material starts to saturate, the eddy current losses are reduced because they also saturate. Since the eddy current losses are a function of $d\phi_B/dt$, as the material saturates, the rate of change of B, and therefore ϕ, also decreases reducing the induced currents. In [10] a circuit model for SPICE simulation is presented that includes the small signal inductance and losses, along with the change of inductance and resistance as a function of the DC current. But since this is a small-signal model with DC superposition, the large signal or hysteresis losses are not included.

Air core inductors, as shown in [3], have been used at very high frequencies above 100 MHz with the advantage of the elimination of magnetic losses. Thin-film inductors, as shown in [11, 12, 13, 14, 15, 16, 17], have been used for frequencies above 10 MHz with inductance in the range of 10 nH to 50 nH and DC resistance in the range of 20 mΩ to 300 mΩ. For input voltage of 12 V or above, the switching losses prevent the converter to operate above a few MHz, with a typical frequency range of 250 kHz to 2 MHz. At 2 MHz and a current ripple of 0.5 A, the required inductance would be 450 nH. For Point-of-Load regulators that operate at 2 MHz or below, PCB embedded inductors have been proposed in [18] and [19] with inductance over 600 nH and inductance density between 3 to 7 nH/mm^2. Figure 1.7 shows several embedded inductor technologies published in the last decade.

In the review paper [30], several types of inductors and magnetic materials are surveyed and compared using DC and AC performance metrics, exposing their advantages and weaknesses. The review paper also concluded that for high-performance integrated power modules a system co-design between inductors, power stage topologies, packaging, and thermal management is required.

For the inductor fabrication, we observed that there are basically three ways they can be manufactured: i) using copper-on-magnetic (CM) or magnetic-on-copper (MC) as in

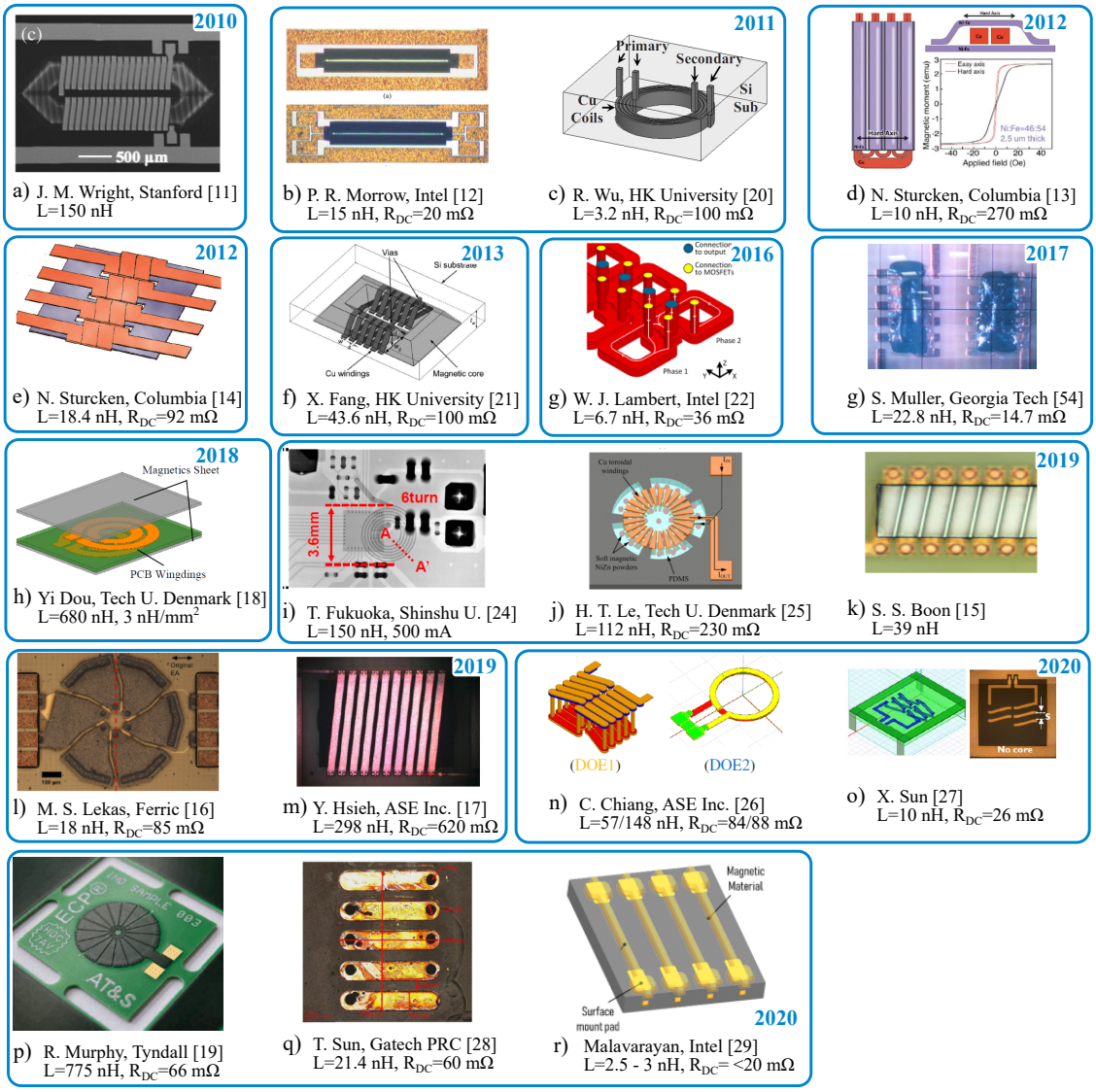


Figure 1.7: Survey of embedded inductors for IVRs.

the case of spiral inductors, ii) magnetic-copper-magnetic (MCM) as in the case of race-track, strip-line, and spiral inductors, iii) and copper-magnetic-copper (CMC) as in the case of solenoid and toroidal inductors. For the coils, they can be fabricated by additive or subtractive manufacturing, also in some cases, the coils are fabricated using bonding-wires [31].

1.3 Buck Converters

Integrated voltage regulators are built using switched inductor topologies in a configuration known as buck converter. A low output voltage is produced from a higher one with very high efficiency. Switched inductor buck converters are used due to their simple circuit topology and their higher efficiency compared to other circuits that use only switched capacitors or linear regulators. The simple buck converter, along with its two switching states and the inductor current waveform, is shown in Figure 1.8.

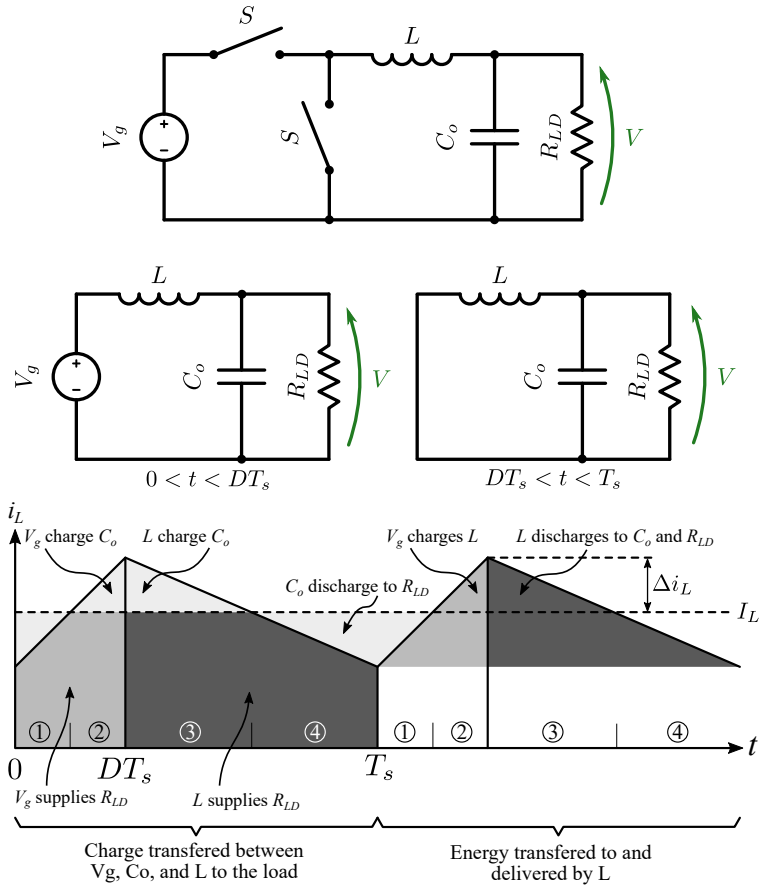


Figure 1.8: Simple buck converter showing its two switching states and the inductor current ripple waveform.

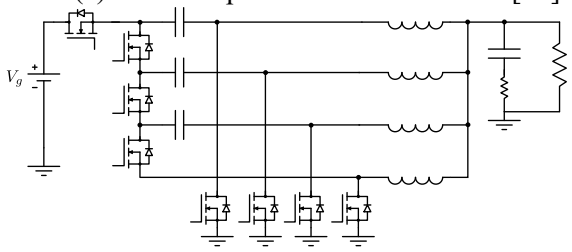
During the first state, when $0 < t < DT_s$, the high-side switch is closed, the low-side switch is open, and the source is connected through the inductor to the load. During the second state, when $DT_s < t < T_s$, the high-side switch is open, the low-side switch is

closed, the source is disconnected, and the inductor is placed in parallel to the load. Here $0 < D < 1$ is the duty cycle and T_s is the switching period. In the first half of the first state (sub-interval 1) both the source V_g and the output capacitor C_o supplies current to the load, while the inductor L is being charged by V_g. In the second half of the first state (sub-interval 2) the source V_g charges both C_o and L while it also supplies energy to the load. In the first half of the second state (sub-interval 3) the inductor completes charging C_o, while at the same time it supplies current to the load. During the second half of the second state (sub-interval 4) both C_o and L supplies energy to the load. This process of exchange of energy repeats continuously with a period T_s. As result, the average voltage developed at the output is approximate DV_g.

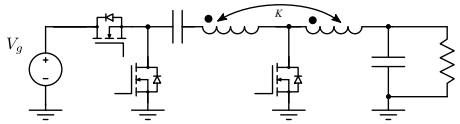
In this exchange of energy between the voltage source, inductor, and load, some energy is lost in the process by two main mechanisms: by active losses due to switching transitions in the MOSFET and by conduction and magnetic losses due to parasitics effects on components. As will be shown later, the main sources of active losses are the output capacitance (between source and drain) and the gate charge (charge required to turn the device on/off) of the transistors.

Other topologies exist that introduce modifications to reduce the active losses. A series capacitor buck converter [32], as shown in Figure 1.9(a), uses switched capacitors with inductors to reduce the voltage stress over the MOSFETs. In this topology, the duty cycle is extended by an integer factor k, where k is the number of phases, by effectively changing the voltage seen by each phase by a factor of $1/k$. However, in this topology the flying capacitor adds series resistance, and the low side switch (rectifier switch) contributes more with its on-resistance as it is shared by adjacent phases. The topology presented in Figure 1.9(b) [33] combines a series capacitor along with a tapped inductor to build a resonant tank between the capacitor and leakage inductance of the tapped inductor, so the MOSFET can be soft switched reducing their losses. The tapped inductor also increments the conversion ratio and extends the duty cycle. The hybrid topology in Figure 1.9(c) [34]

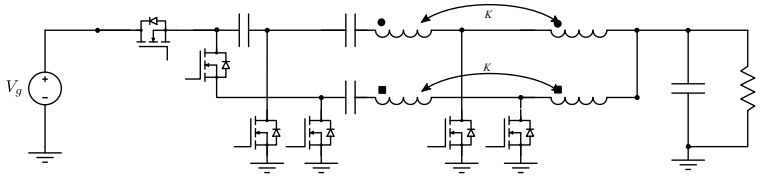
(a) Series Capacitor Buck Converter [32]



(b) Series Capacitor Tapped Inductor Buck Converter [33]



(c) Hybrid Series Capacitor Tapped Inductor Buck Converter [34]



(d) Hybrid ZVS Buck Converter for 12V to 1V [35]

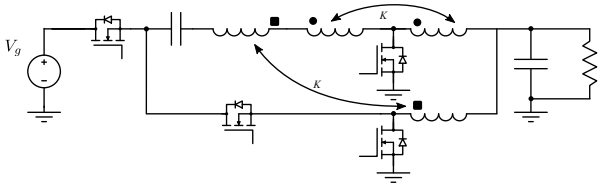


Figure 1.9: Review of Power Stage Topologies.

combines the series capacitor [32] with the tapped inductor [33] to further provide an ultra-high conversion ratio. In Figure 1.9(d) [35] a topology for 12V to 1V is presented that uses a coupled inductor with a turn ratio of $n = n_p/n_s = 2$ to extend the duty cycle close to 0.5, which is the optimal point, but with a non-linear duty cycle to output voltage relation.

Regarding its fabrication, we can identify three main types of voltage regulators: i) voltage regulator modules that consist of power supplies built on a PCB board or as discrete modules to be mounted on a PCB, ii) package voltage regulator that corresponds to power supplies built on the SoC package, and iii) chip voltage regulator where all the components (inductors, capacitor, controllers, switches, etc.) are built in the same silicon. The last two categories are also known as Integrated Voltage Regulators. As expected, as the solution size decrease from VRMs to IVRs, the complexity increases.

To compare these integration strategies, we first use the next Figure of Merit (FoM), with Figure 1.10 showing the plot of several surveyed publications.

$$FoM = f_{sw} \cdot \frac{V_{in}}{V_{out}} \cdot V_{in} \cdot \frac{I_{out}}{\text{volume}} \tag{1.15}$$

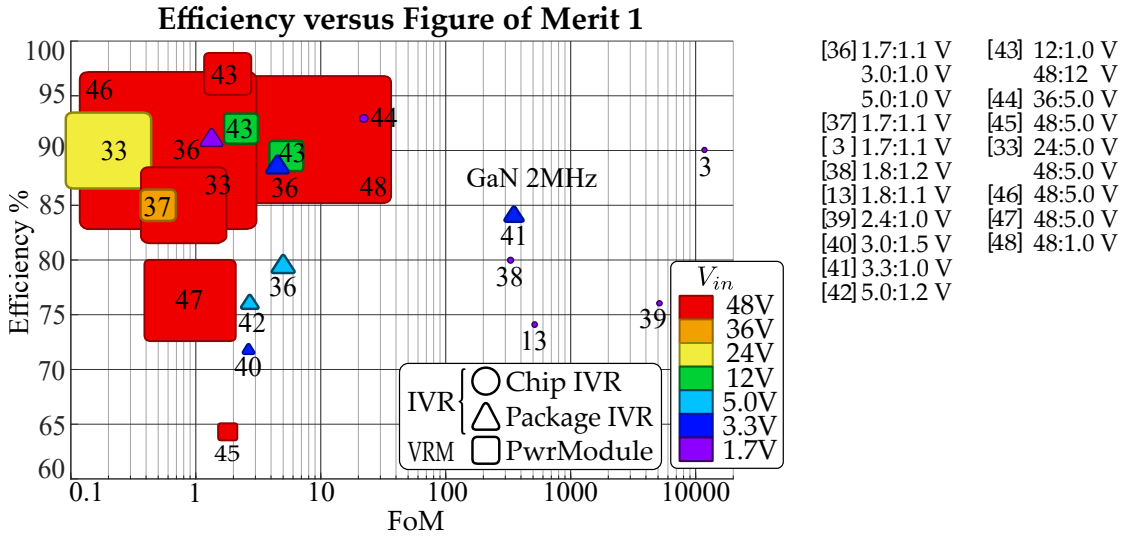


Figure 1.10: First Figure of Merit of Voltage Regulators.

In the Figure 1.10 FoM plot, the shape corresponds to the type of solution, the shape size to its relative size to other modules, the shape color is the input voltage, and the number is the bibliography reference. We can distinguish three categories: i) low voltage less than 1.7V, ii) medium voltage between 3.3V to 5V, and iii) high voltage from 12V to 48V. Only VRM can handle voltage over 12V while IVR only works with voltages below 5V.

But when comparing different power modules with different conversion ratios, the use of frequency in the figure of merit can be misleading. What matters the most is the power density for a given conversion ratio versus efficiency. Higher frequency implies better bandwidth only when comparing two solutions with similar conversion ratios, density, and efficiency. To be able to compare different types of converters the next FoM is used instead:

$$FoM = \frac{V_{in}}{V_{out}} \cdot V_{in} \cdot \frac{I_{out}}{\text{volume}} \tag{1.16}$$

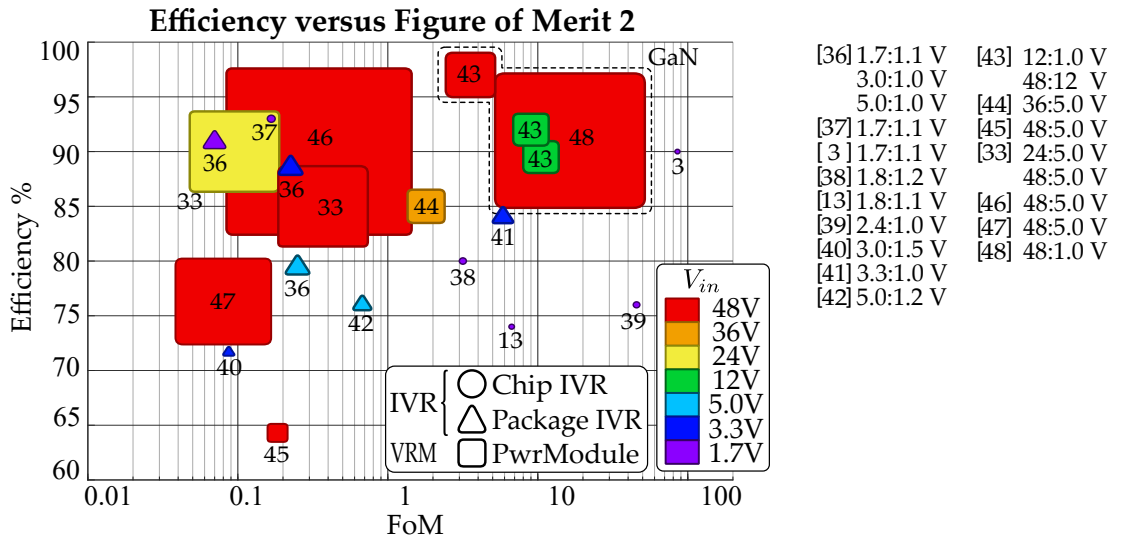


Figure 1.11: Second Figure of Merit of Voltage Regulators.

As can be seen from Figure 1.11 using this other FoM, design high conversion ratio converters in a small package is as complex as a highly integrated low voltage converter that works at very high frequencies. In high-voltage low-frequency voltage regulator the complexity is due to i) losses increase with the square of input voltage, and ii) high inductance density with high saturation current and low DC resistance is difficult to achieve. In low-voltage high-frequency converters the complexity is due to: i) the switching losses increase linearly with frequency, and ii) inductor losses increase with the frequency as well.

1.3.1 Low Voltage IVRs

Extensive research has been done for embedded inductors and IVRs, mostly for low input voltage ($V_{IN} \leq 5$ V) with a typical conversion ratio of 1.7 V to 1 V. With low input voltages it is possible to use higher switching frequencies because low voltage MOSFETs have lower parasitic capacitance and losses. With a conversion ratio of 1.7 V to 1 V at frequencies above 10 MHz, the required inductance can be lower than 35 nH. Table 1.1 shows a list of publications and commercial IVRs along with their key properties.

As the table shows, most of the low voltage IVRs are designed at frequencies above 100 MHz to take advantage of the required low inductance. However, the conversion ratio is

Table 1.1: Low voltage IVR comparison table.

Ref.	Year	V_{IN} [V]	V_{OUT} [V]	I_{OUT} [A]	L [nH]	f_{sw} [MHz]	Eff. [%]
[49]	2011	1.2	0.86	0.150	2	200	77
[13]	2012	1.8	1.1	3.0	5.9	75	74
[50]	2013	1.2	0.9	0.370	5.5	100	83.2
[3]	2014	1.7	1.05	NM	$<$10	140	90
[38]	2015	1.66	0.83	0.39	12	150	82
[51]	2016	1.6	1.1	6	2	150	89
[37]	2016	1.7	1.0	0.8	2.1	200	93
[42]	2018	5	1.2	0.6	NM	4	84

limited to an input voltage of 1.8 V or less. The commercial product from Altera EN5322QI [42] supports an input voltage of 5 V and operates at 4 MHz, a considerable difference with respect to the rest of 1.7 V input IVRs.

1.3.2 High Voltage IVRs

To reduce the losses in a conventional hard switched buck converter, switched capacitors are combined with inductors to form a hybrid buck converter. In [52] several hybrid converters for 48 V to 1 V are surveyed explaining their frequency, duty cycle, and efficiency limitation. What the hybrid topologies have in common is that they use switched capacitors along with the inductors to reduce the voltage stress and losses over the MOSFET and additionally extend the duty cycle. As shown in the survey, a switching frequency of 2 MHz can be achieved for 48 V to 1 V and 12 V to 1V. For input voltages of 5 V or more, most of the voltage regulators are discrete or on-board solutions. Table 1.2 shows some published works for 12 V to 1 V and 48 V to 1 V.

As the table shows, most of the voltage regulators for high voltage input works with frequencies below 1 MHz with high inductance values. Also, most of them use hybrid solutions and tapped-inductors or transformers (Tr).

Table 1.2: High voltage IVR comparison table.

Ref.	Year	V_{IN} [V]	V_{OUT} [V]	I_{OUT} [A]	L	f_{sw}	Eff. [%]
[46]	2014	48	5	10	2:1 2.25 uH Tr	750 kHz	90
[48]	2016	48	1	50	2x250 nH + 5:1 Tr	600 kHz	88
[45]	2016	48	5	0.2	500 nH	10 MHz	81
[44]	2017	36	6	3	NA	275 kHz	85
[43]	2018	12	1	12	250 nH	1 MHz	89
[43]	2018	48	12	15	4.7 uH	500 kHz	97
[33]	2018	24	5	3	1:1 220 Tr	3 MHz	90
[47]	2018	24	5	0.5	1.5 uH	9-15 MHz	76.3

1.3.3 Si and GaN MOSFETs

Silicon MOSFETs have been the fundamental semiconductor block for Point of Load (PoL) voltage regulators. Si MOSFETs allow building on the same IC both the switches and control circuitry. However, Si MOSFETs have very large switching losses due to its parasitic capacitance, slow on-off transition, and body diode reverse recovery charge. For high voltage applications, with voltages greater than 12 V, Gallium-Nitride (GaN) MOSFETs show a better performance. Table 1.3 shows the basic properties of Si and GaN semiconductors [53].

Table 1.3: Silicon and GaN key properties.

Parameter	Units	Silicon	GaN
Band Gap E_g	eV	1.12	3.39
Critical Field E_{Crit}	MV/cm	0.23	3.3
Electron Mobility μ_n	$cm^2/V \cdot s$	1400	1500
Permittivity ϵ_r		11.8	9

Higher band gaps mean electrons are harder to move from one state to another, this reduces the leakage current and allows a higher operating temperature. A higher critical field allows having a higher breakdown voltage V_{BR} in a smaller size, also reducing parasitic capacitance for high voltage devices. The higher electron mobility produces lower on-resistance, and a higher critical field allows a shorter channel length further reducing

the channel resistance. The theoretical channel on-resistance $R_{DS(on)}$ is given by [53],

$$R_{DS(on)} = \frac{4V_{BR}^2}{\epsilon_0 \epsilon_r E_{Crit}^2} \tag{1.17}$$

As result, the theoretical limit for the resistance is much lower for GaN MOSFET compared to Si MOSFET. The parasitic capacitance, because of size reduction, is also smaller for GaN MOSFET.

1.4 Buck Converter Breakdown Losses

As discussed in the previous sections, the main three types of losses in a hard switched buck converter are the conduction losses of the MOSFET and inductor, the inductor AC magnetic losses, and the MOSFET dynamic, or switching, losses. The conduction losses P_{cond} are due to the non-zero resistance of each component, and is given by the next expression,

$$P_{cond} = \left(I^2 + \frac{\Delta i^2}{3} \right) (DR_{HS} + (1-D)R_{LS}) + I^2 R_{L,DC} \tag{1.18}$$

where D is the converter duty cycle, R_{HS} and R_{LS} are the MOSFET high-side and low-side on-resistance, I is the inductor DC current, and Δi_L is the inductor current ripple. The inductor AC losses P_{AC} are produced by the contribution of all current ripple harmonics on the inductor copper windings, eddy currents induced in the magnetic materials, and magnetic hysteresis losses. The expression for these losses is more elaborated and will be given in the following chapters.

The Gallium-Nitride (GaN) FET switching losses are [53]: the gate charge losses P_G, turn-on and turn-off losses P_{IV}, output capacitance losses P_{oss}, and reverse conduction losses P_{SD}. The most dominant losses in a high-voltage buck converter are the conduction and output capacitance losses, with the latter given by the next expression,

$$P_{oss} = \int_0^{V_{IN}} v_{DS}\, C_{DS}(v_{DS}) \cdot dv_{DS} \cdot f_s \propto V_{IN}^2 \cdot f_s \tag{1.19}$$

where v_{DS} is the voltage across the drain and source, C_{DS} is the output capacitance and is a function of v_{DS}, and f_s is the switching frequency.

These three major loss contributions, along with all other loss sources, are breakdown and plotted in Figure 1.12 as a function of frequency. It was considered an input voltage $V_{IN} = 48$ V, output voltage $V = 1$ V, duty cycle $D = 2.36$ %, inductance $L = 338$ nH, inductor DC resistance $R_{DC} = 15$ mΩ, and DC inductor current of $I = 2.5$ A.

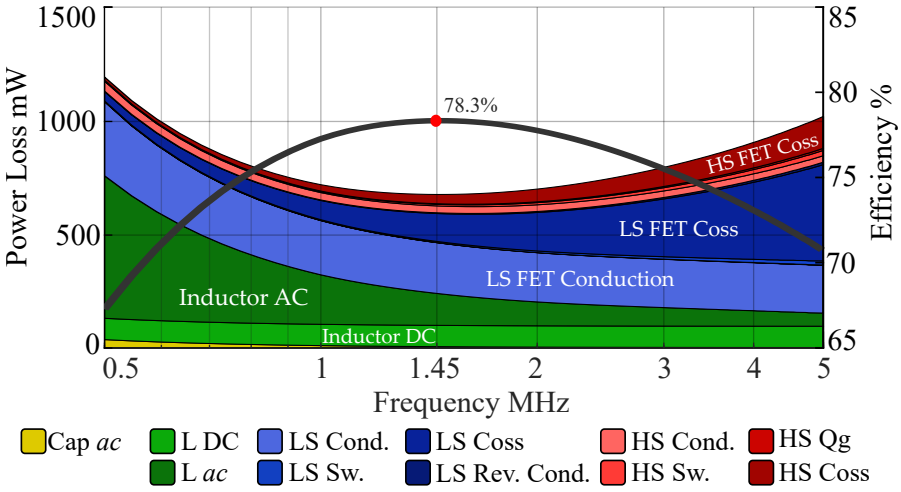


Figure 1.12: IVR loss breakdown.

When a series capacitor topology is used, the voltage across the MOSFET is reduced by a factor equal to the number of phases, and the duty cycle increase by the same factor. In this way, with $V_{IN} = 48$ V, using 2 phases we have $V_{DS} = 24$ V and $D = 5$ %, and with 4 phases we have $V_{DS} = 12$ V and $D = 10$ %. Figure 1.13 shows the resulting power loss breakdown in these two scenarios. As this loss breakdown shows, as the number of phases increases the output capacitance losses are reduced, but also the conduction losses are increased. More than 4 phases become impractical, and little gain in terms of efficiency.

From the breakdown losses, we see that the frequency for maximum efficiency goes from 1.5 MHz single phase to 3 MHz when two or four phases are used.

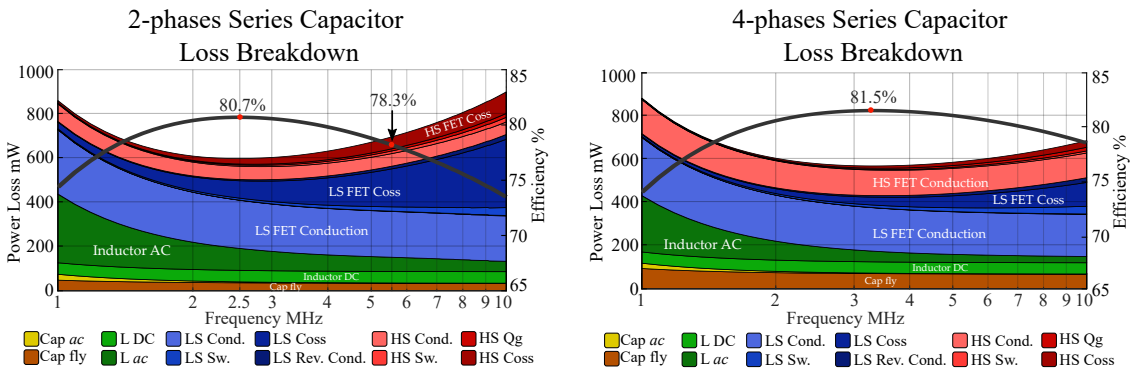


Figure 1.13: Series Capacitor IVR loss breakdown.

1.5 Thesis Goal and Structure

To achieve high inductance values one or more of the next options are required: increase size, increase the number of coil turns, or increase the material permeability. But each of these options has its drawback. Increase the size is the opposite that is required for IVRs, where the inductor needs to be as small as possible to fit in the IVR package. Increase the number of turns also increases the size and the DC resistance reducing the inductor efficiency. Increase the permeability also increases the magnetic losses and reduces the saturation current. And in general, anything that is done to increase the inductance density also reduces the saturation current and limits how much power the IVR can deliver.

The fabrication process to build new inductor structures can be difficult to realize or optimize. Therefore, the inductor design must be guided by the fabrication capabilities, this is called Design for Manufacture, or DFM. Some clever inductor structures may not be manufacturable, leaving them as just nice models.

Finally, in a buck converter, the inductor excitation is not sinusoidal, making most of the methods to calculate the inductor losses far from accurate. Moreover, most of the methods have only been characterized in the kHz range. Since the inductor is part of a bigger system, its properties also need to be matched to the working conditions of the buck converter. For instance, if the buck converter is limited to a maximum frequency of 2 MHz, it is of no use a good inductor at 5 MHz but without enough inductance to operate at 2 MHz. On the

other hand, an inductor with enough inductance at 2 MHz can have very high losses at 5 MHz. It becomes very challenging to trade off all the possibilities.

All these issues need to be addressed to determine what can be improved and what are the fundamental limits that prevent the inductors for high-voltage and high-conversion ratio IVR possible. Based on these challenges, this thesis works on three main goals: i) develop a new embedded inductor technology for high conversion ratio IVR with very low DC resistance and high inductance density, ii) develop a new method for the inductor power loss calculation that allows for easier and more accurate estimation considering the duty cycle effect and frequency in the MHz range, and iii) evaluate different magnetic materials to determine the properties required to make a single-stage high-voltage IVR possible.

This thesis is structured as follows. Chapter 2 shows the structural design and requirements for embedded inductors to work. It starts by analyzing the performance of solenoids and toroids when they are embedded, to then explore the geometrical possibilities that magnetic sheets offer to build them.

Chapter 3 presents the theoretical development for the new inductor power loss calculation method which is then used to determine the required properties in terms of inductance and resistance. It also presents the measurement setup used to validate the presented ideas.

Chapter 4 presents the inductor fabrication process and results, including all the measurements and the large to small losses relation.

Chapter 5 shows a small-signal SPICE circuit model that allows an easy extrapolation of inductor models with any amount of inductance.

Chapter 6 presents a way to use a simple discrete toroidal inductor to predict the losses of more complex embedded ones. This analysis also allows determining the magnetic properties of the required magnetic material to make high conversion ratio IVRs possible.

Chapter 7 finalizes with a conclusion of the work presented in this thesis.

1.6 Summary

The power delivery network requirements, for next-generation computing platforms, are challenging to be met with current multi-stage power conversion. A typical multi-stage 48 V to 1 V down conversion system shows an efficiency of 75% or less. By powering the SoC with a higher voltage than 1.7 V (as used by today's packages), the routing losses can be greatly reduced increasing the efficiency, and at the same time, increasing the regulation bandwidth.

Voltage regulators that take the task of performing the voltage down conversion to the same SoC package are called Integrated Voltage Regulators or IVR. IVRs required high-performance embedded passive components such as capacitors and inductors. However, for high-voltage IVRs it becomes very challenging to fabricate low loss and high-density inductors. As the input voltage increases, the converter switching frequency reduces requiring higher values of inductance. Inductors fabricated with magnetic materials give the possibility to increase the inductance, but a trade-off exists between how much energy can be store and the inductor size. By using more complex circuit topologies and multiple voltage regulation phases, it is possible to reduce the apparent voltage seen by the inductor reducing the required amount of inductance.

Most of the IVR published in the literature works at low input voltages (typically 1.7V) and very high frequencies around 100 MHz. In this way, only a small amount of inductance of less than 5 nH is required. However, this cannot be scaled for greater input voltages. For input voltages of 12 V to higher, the switching frequencies are kept below 5 MHz to reduce the MOSFET losses. At 5 MHz the required inductance can be greater than 160 nH. The limitation of frequency is given by the parasitic capacitances of the MOSFETs, where the losses increase linearly with the frequency and with the square of the voltage across the MOSFET.

This thesis aims to develop a new inductor technology along with a design framework.

This design framework is based on a new inductor power loss calculation method that only relies on simple circuit quantities such as inductance and current, instead of magnetic fields as typically used by other methods. To validate the inductor model and framework, several inductors and materials are demonstrated and characterized, allowing to know the research roadmap for the required magnetic material.

CHAPTER 2

EMBEDDED INDUCTORS FOR IVR

The increased demand in computational capacity and size miniaturization for emerging electronic devices are setting new levels of efficiency and thermal constraints on power delivery systems. System on Package (SOP) solutions require converters with a switching frequency in the range of 10-100 MHz to reduce the inductance value and the inductor footprint to allow their integration closer to the switching devices. Nevertheless, for input voltages above 12V, the frequency has been kept below 10 MHz to obtain high-efficiency levels, but requiring higher values of inductance.

IVR integration remains a challenging problem, with a major bottleneck being the integration of power inductors especially for high-efficiency and high-conversion ratio converters, in applications such as personal computers and servers where conversion ratios of 12:1V or 48:1V (with currents of 10A - 200A) are typical. A better approach for inductor integration is by embedding it in the substrate, just underneath the active circuitry. This allows better usage of the available package volume as shown in Figure 2.1. When the inductor is placed on-surface, its size needs to be as small as possible setting several constraints on the minimum value for DC and AC resistances, and inductance. However, when the inductor is embedded we just need to make it small enough to fit underneath the rest of the module, leaving more optimization space to lower the inductor losses.

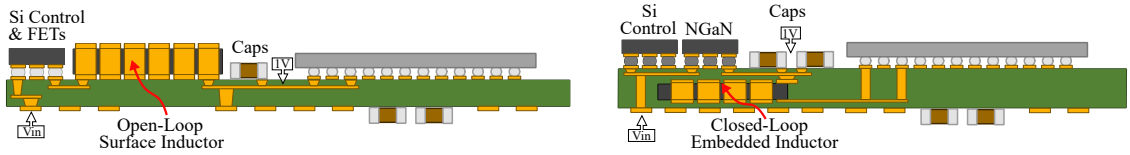


Figure 2.1: Inductor integration strategies. (left) Surface inductor. (right) Embedded inductors for high-density heterogeneous integration.

In this chapter, we show the impact of surrounding conducting surfaces, such as power

planes, on package-embedded solenoidal inductors where the inductance can decrease by more than 35%. Then, we present a closed-loop toroidal design that shows a minimal impact on inductance when embedded. This leads to an inductor design exploration where a novel structure is presented.

2.1 Surface and Embedded Inductors

To explore the effect of conduction planes around the inductor, an inductor was designed for an inductance around 35nH at 10 MHz using NiZn magnetic composite material, which was previously developed at Georgia Tech [54].

The magnetic material properties, such as the relative permeability μ_r' and magnetic loss tangent $\tan\delta_m$, as a function of frequency are shown in Figure 2.2, where the complex permeability is defined as follows,

$$\mu = \mu' - j\mu'' = \mu'\left(1 - j\frac{\mu''}{\mu'}\right) = \mu_0\mu_r'(1 - j\tan\delta_m) \tag{2.1}$$

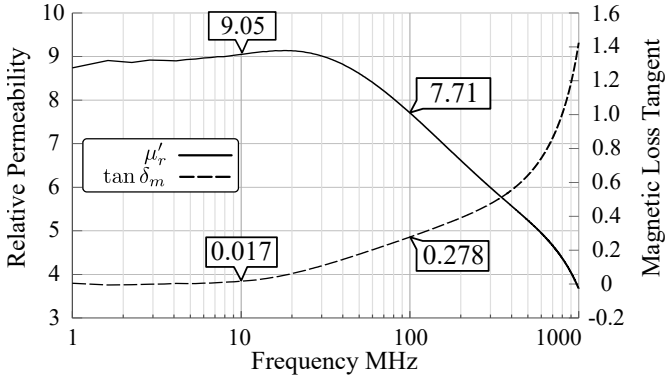


Figure 2.2: NiZn ferrite composite magnetic material properties.

Two inductor structures were designed: solenoid (open-loop) and toroid (closed-loop) as shown in Figure 2.3. Also, each structure was simulated with a different number of turns.

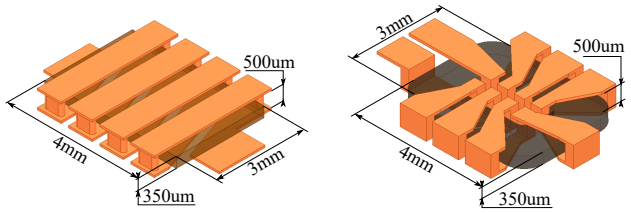


Figure 2.3: Solenoidal and toroidal inductor models.

Assuming ideal solenoid and toroid structures, as shown in Figure 2.4, the inductance can be found by solving for the flux $\phi(t)$ enclosed by the windings and can be approximated by,

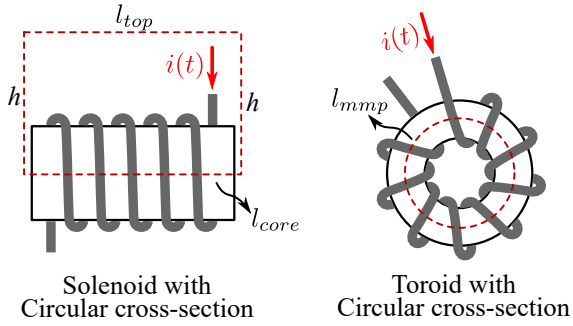


Figure 2.4: Ideal Solenoidal and toroidal inductors.

$$\int_C \vec{H} \cdot dl = H\, l = N\, i(t)$$

$$\phi(t) = \mu_0 \mu_r' \int_S \vec{H} \cdot dA = \mu_0 \mu_r' \frac{N\, i(t)}{l} A$$

where N is the number of turns, l is the path for the contour integral which is l_{core} for the solenoid and l_{mmp} for the toroid, and the magnetic field intensity $\vec{H}$ was considered uniform over the integration path and surface. In the solenoid, we can always set the length h in the magnetic path arbitrarily large so that the contribution of $\vec{H} \cdot dl$ vanish, and only l_{core} contribute. The surface integral is over the cross-sectional area of each structure.

We can now express the developed voltage $v_L(t)$ across the inductor as a function of

the inductor current $i(t)$ as follows,

$$v_L(t) = N\frac{d\phi}{dt} = \mu_0\mu_r'\frac{N^2A}{l}\frac{di}{dt} \tag{2.2}$$

to obtain the inductance given by equation (Equation 2.3).

$$L_{dsn} = \mu_0\mu_e'\frac{N^2A}{l} \tag{2.3}$$

where μ_r' from (Equation 2.2) was replaced by μ_e' to adjust the permeability as it is lower because of demagnetization effect, shape anisotropy, and partial filling with magnetic material. This parameter μ_e' can be used to estimate the usage factor of the magnetic material. The approximated inductance values for both the solenoid and toroid are given in Table 2.1.

Table 2.1: Inductor design parameters at $f_s = 10$MHz.

	Solenoid			Toroid		
	3 Turns	4 Turns	5 Turns	6 Turns	8 Turns	10 Turns
L_{dsn}	16.8 nH	29.9 nH	46.8 nH	15.0 nH	26.6 nH	41.6 nH
L_{air}	3.8 nH	6.8 nH	10.7 nH	4.4 nH	7.8 nH	12.1 nH
μ_e'		4.38			3.43	

To extract the inductance from simulation (or measured data), the simple inductor model shown in Figure 2.5 can be used. The RLGC parameters are extracted from S-Parameters, which are converted to either Z or Y parameters, and are given by the formulae (Equation 2.4) to (Equation 2.5).

$$R = -Re\left\{\frac{1}{Y_{21}}\right\}, \quad G = Re\left\{\frac{1}{Z_{11}+Z_{21}}\right\} \tag{2.4}$$

$$L = -Img\left\{\frac{1}{\omega Y_{21}}\right\}, \quad C = Img\left\{\frac{1}{\omega(Z_{11}+Z_{21})}\right\} \tag{2.5}$$

It was found that the calculated values for R,L,G,C are more accurate if R and L are

computed using the Y-Parameters, and G and C computed from the Z-Parameters where Z and Y are obtained from S-parameters.

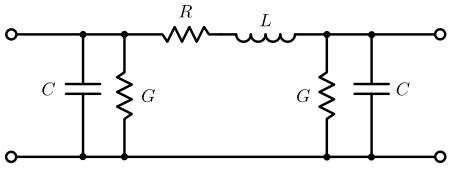


Figure 2.5: Inductor model for RLGC parameter extraction.

In practical terms, only R and L are relevant. The parameters C and G are more dependent on the position of the inductor with respect to the ground or power plane and can be usually neglected. Later in Chapter 5, a more accurate inductor model is presented.

2.1.1 Embedded Solenoid

Through simulation of the inductor structures, we obtained for the solenoid the inductance against the frequency with 3, 4, and 5 turns as shown in Figure 2.6. From the figure, we see that when the inductor is embedded (placed between two conducting planes) the inductance drops significantly. This also affects the quality factor Q.

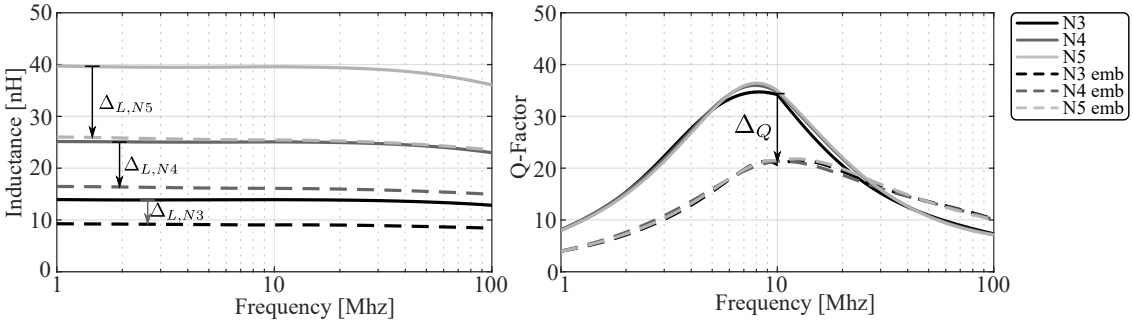


Figure 2.6: Solenoidal inductor inductance vs frequency.

Table 2.2 summarizes the solenoid inductor characteristics, where L and L_{air} are the inductance with and without the magnetic material, respectively. From the table, we see that both the inductance and Q-factor drop by more than 35% compared to the on-surface inductor values. This makes a solenoid structure unsuitable for high heterogeneous inte-

gration density, where the inductor must be placed embedded and underneath the active circuitry and power stage, as shown in Figure 2.1.

Table 2.2: Solenoidal inductor parameters at $f_s = 10$MHz.

	3 Turns		4 Turns		5 Turns	
	Surf.	Emb.	Surf.	Emb.	Surf.	Emb.
L	13.9 nH	9.1 nH	25.1 nH	16.1 nH	39.6 nH	25.4 nH
L_{air}	4.5 nH	3.9 nH	7.9 nH	6.8 nH	12.3 nH	10.7 nH
Δ_L	34.9%		35.8%		35.7%	
μ'_e	3.12	2.34	3.18	2.37	3.22	2.38
R_{DC}	5.3 mΩ		9.9 mΩ		16.8 mΩ	
R_{AC}	26 mΩ	27 mΩ	45 mΩ	47 mΩ	71 mΩ	75 mΩ
Q	34.2	20.7	34.7	21.3	35.0	21.4
Δ_Q	39.4%		38.6%		38.7%	

In Figure 2.7 both solenoid inductor scenarios – surface and embedded – are depicted, where, with the plotted H-field, it can be seen that the conduction planes reduce the field intensity, and decreasing the inductance.

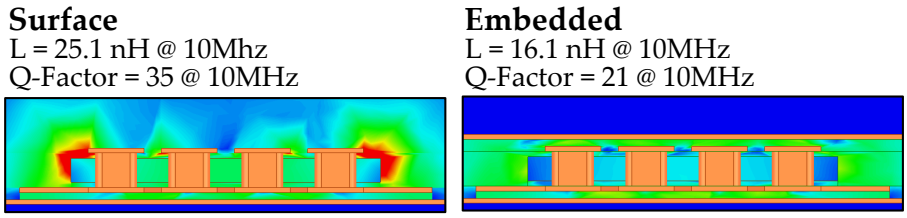


Figure 2.7: Surface and embedded solenoidal inductor H-Field.

2.1.2 Embedded Toroid

For the toroid, Figure 4.5 shows the inductance against frequency for the inductor with 6, 8, and 10 turns. From the figure we see that when the inductor is embedded the inductance does not drop as significantly as compared to the solenoid, but also it is higher. The Q-factor is also not greatly affected.

Table 2.3 summarizes the toroidal inductor characteristics. From the parameter μ'_e we see that the magnetic material usage is higher when it is embedded. In addition, from the

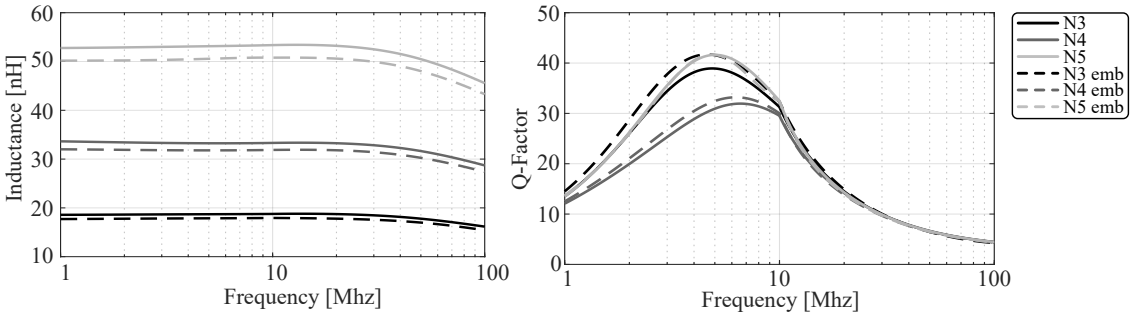


Figure 2.8: Toroidal inductor inductance vs frequency.

table, we see that the DC characteristic is almost the same as the solenoid, but when it is embedded it out-performs the characteristics of the solenoidal structure.

Table 2.3: Toroidal inductor parameters at $f_s = 10$MHz.

	6 Turns		8 Turns		10 Turns	
	Surf.	Emb.	Surf.	Emb.	Surf.	Emb.
L	18.8 nH	17.9 nH	33.3 nH	31.9 nH	53.4 nH	50.8 nH
L_{air}	5.0 nH	4.4 nH	8.3 nH	7.6 nH	13.3 nH	12.3 nH
Δ_L	4.393%		4.317%		4.821%	
μ'_e	3.78	4.06	4.02	4.21	4.01	4.12
R_{DC}	5.1 mΩ		9.7 mΩ		16.3 mΩ	
R_{AC}	38 mΩ	35 mΩ	71 mΩ	67 mΩ	103 mΩ	99 mΩ
Q	31.3	32.3	29.5	30.0	32.5	32.4
Δ_Q	3.229%		1.577%		0.234%	

In Figure 2.9 both toroidal inductor scenarios – surface and embedded – are depicted, with the plotted H-field it can be seen that the conduction planes do not have a significant impact on the field intensity, since most of the energy is stored inside the toroid.

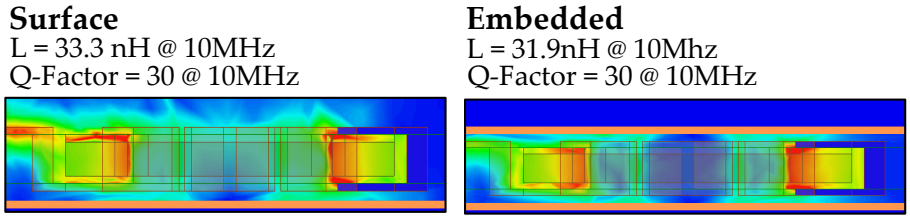


Figure 2.9: Surface and embedded toroidal inductor H-Field.

2.2 Embedded Inductors Using Magnetic Sheets

The toroidal inductors presented in the previous section has a low inductance density, only 2.66 nH/mm^3. If instead of using a single magnetic core we use a magnetic sheet with vias thru ferrite the inductance density can be increased, as a result of smaller realizable dimensions. Figure 2.10 shows that a solenoid built on a magnetic sheet also has a closed magnetic path and its inductance is not affected by near conducting planes. Its inductance on surface (L_{surf}) is the same to its inductance (L_{emb}) when embedded.

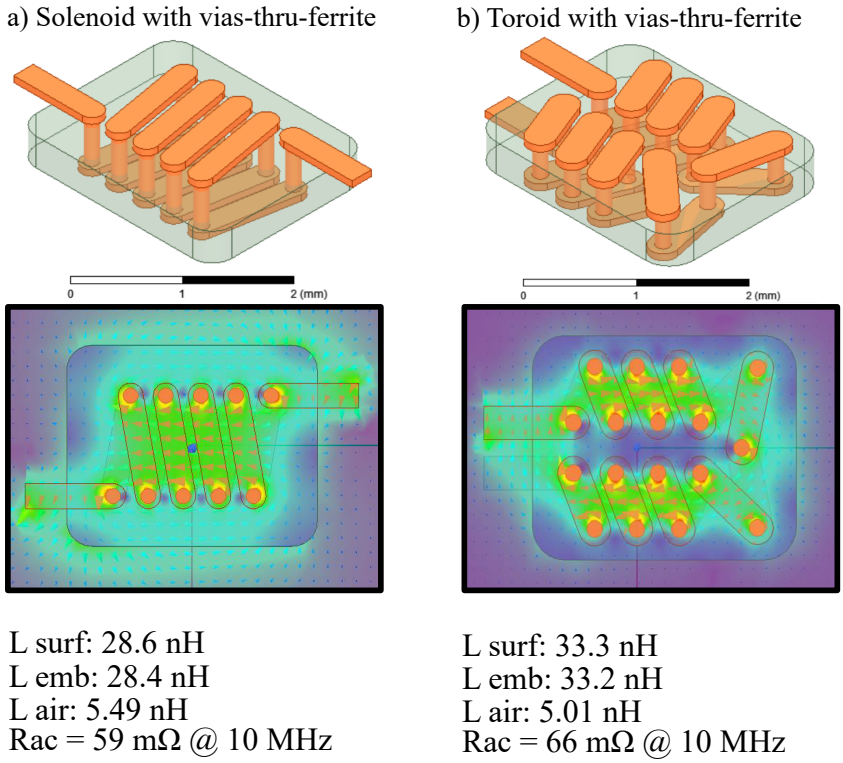


Figure 2.10: Solenoidal and toroidal inductors using magnetic sheet and vias thru ferrite.

Magnetic sheets along with vias thru ferrite allow exploring new inductor structures. The key concept in this type of inductor is that almost all the inductance is built around the vias, and the top and bottom copper are used to connect them and build the inductor cross-sectional area.

2.3 Inductor Structure Design Exploration

Figure 2.11 shows the first set of inductors that were explored. IND014 and IND015 were used to study the inductance on the vias. IND016, IND017, and IND018 were used to study the effect of the magnetic sheets with solenoids and toroids. From IND020 to IND025B

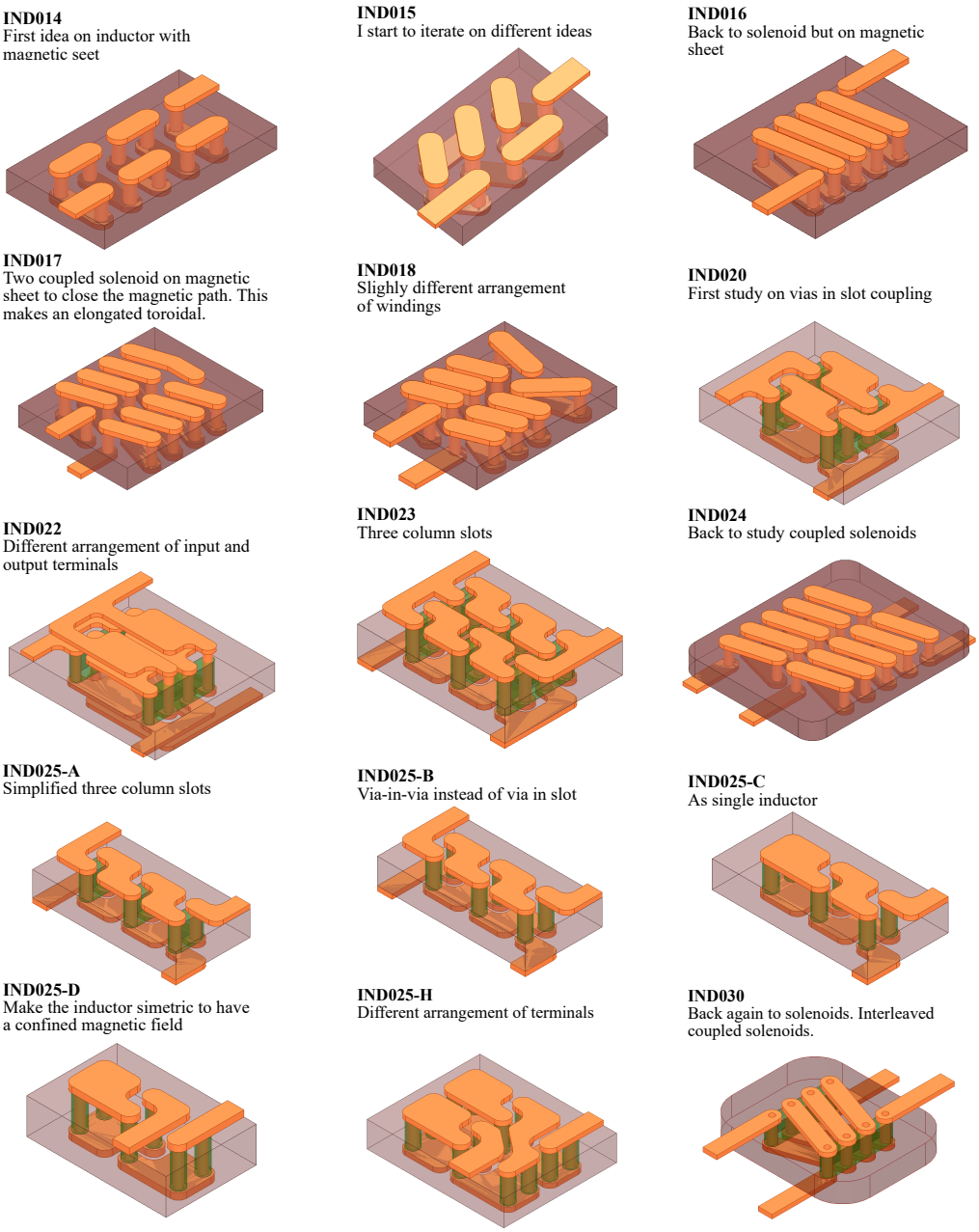


Figure 2.11: Inductor design exploration for first iteration of embedded inductors.

we study the coupling between adjacent and interleaved solenoids using dielectric slots (shown in green). From IND025-C to IND025-H the interleave inductors are merged to form a single inductor. IND030 is another structure for coupled solenoids.

This design exploration results in the concept of incomplete interleaved winding toroidal inductors. Let see this concept from another point of view. Toroidal inductors are complicated to fabricate with many vias and windings as shown in Figure 2.12, limiting the smallest critical dimensions of the inductor. They can be simplified considerably if the windings are arranged longitudinally as shown also in Figure 2.12. They can be thought of as a single incomplete toroidal inductor or two solenoid inductors. They are called incomplete because the winding only covers part of the core.

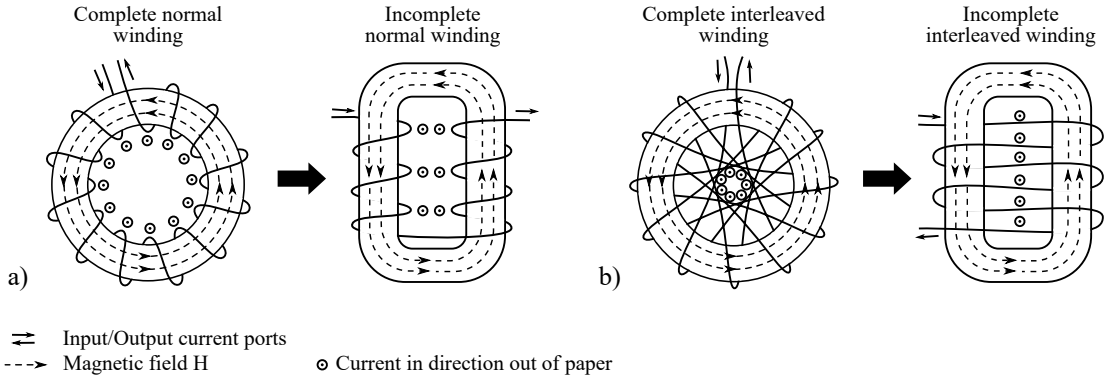


Figure 2.12: Types of toroidal inductor winding.

When the inductor is built using a magnetic sheet as the substrate, both solenoids and toroids show a closed magnetic path. This allows the fabrication of one or more of the inductors eliminating the need to cut discrete magnetic cores. In this work, several configurations derived from the concept shown in Figure 2.12 were fabricated and compared. Figure 2.13 shows several versions of the incomplete interleaved winding toroidal inductor, four of which, IND034, IND035, IND036, and IND037, correspond to the first iteration of fabricated inductors.

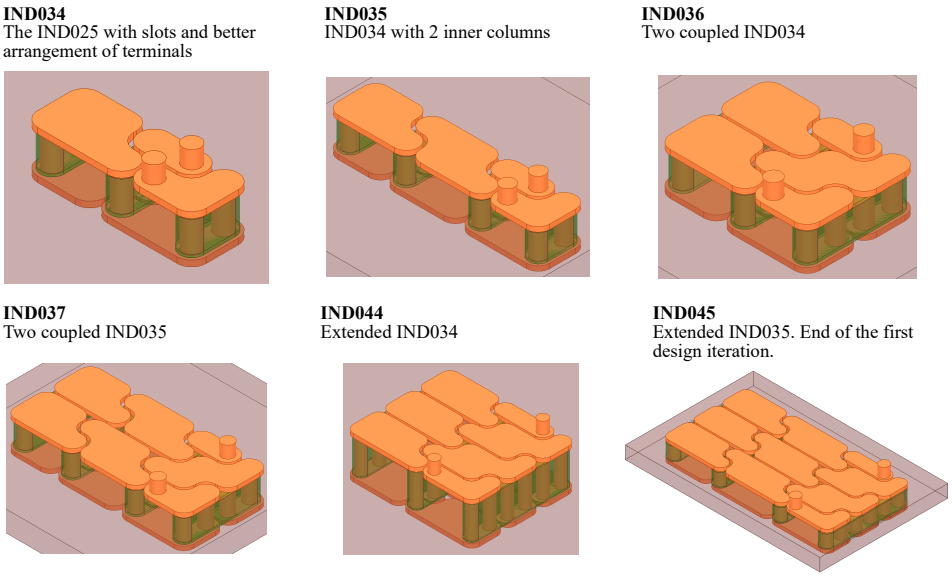


Figure 2.13: Inductor design exploration for the first iteration of embedded inductors.

Let us consider the inductor IND036 which is shown in more detail in Figure 2.14. Several vias are arranged in slots drilled through a magnetic sheet substrate to couple their magnetic field and provide electrical isolation. It has N current elements in the center and $N/2$ current elements on each side. The magnetic field H is built around the central vias with an elongated toroidal field distribution, and the magnetic field is confined to the inductor structure even if the magnetic sheet is much larger. Using Ampere's law $\oint \vec{H} \cdot dl = Ni$, where N is the number of enclosed vias, i is the current through the via, and H is constant along the integration path l_c, we can write the next expresions,

$$2H_c l_c + 2\int_{l_r} H_r dl = 4i \quad \text{and} \quad H_c l_c + \int_{l_e} H_e dl = 2i$$

Solving for $\int_{l_e} H_e dl$ we obtain,

$$\int_{l_e} H_e dl = \int_{l_r} H_r dl$$

and given that $l_e > l_r$, then $H_e < H_r$ outside of the inductor. Far from the inductor H_e becomes very small.

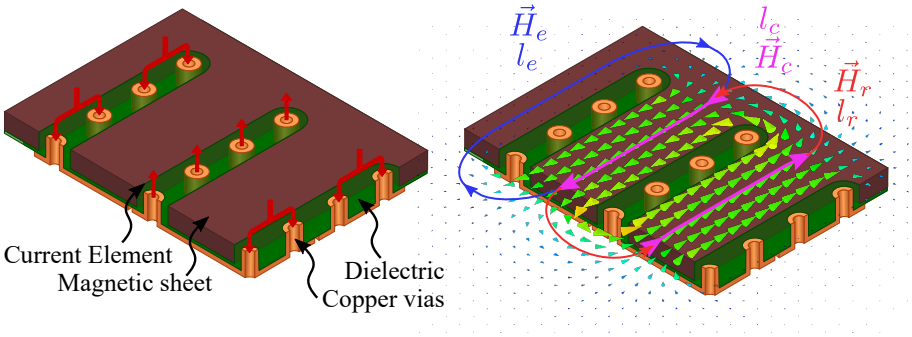


Figure 2.14: Details of inductor current elements distributed in vias.

Figure 2.15 shows the top view of a solenoid (right) and the inductor IND036 (left) in a magnetic sheet size of 2.5 × 2.5 × 0.4 mm, both with the same amount of inductance. The DC resistance for the solenoid is 23 mΩ and for the toroid it is 24.7 mΩ. Figure 2.16 shows the inductance as a function of the substrate width wc. Even though the solenoid seems smaller, its size must be defined according to the space required to build up its inductance, not just its geometrical bounding box. From Figure 2.16 it is observed that the solenoid inductor requires the same space as the IND036, however, the inductor IND036 has more control over the space it will use.

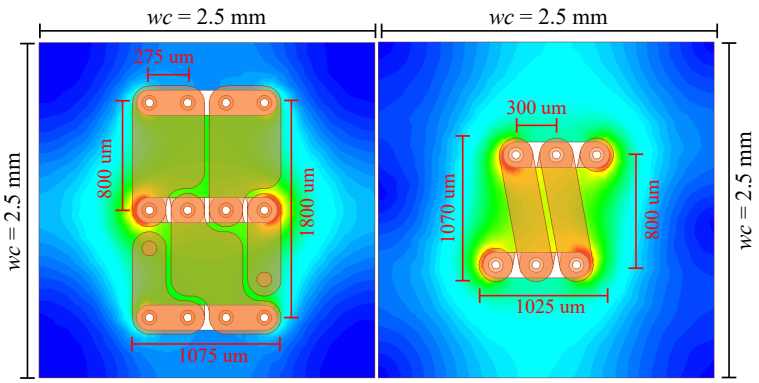


Figure 2.15: Comparison of solenoid and toroid using HBS1 magnetic sheets.

The coupling between inductors in a magnetic sheet can be controlled by the use of slots cut in the magnetic substrate. When the vias of two inductors share the same slot, their coupling is maximized. When the two inductors do not share the same slot, their coupling is minimized. In this way, the coupling between inductors can be controlled.

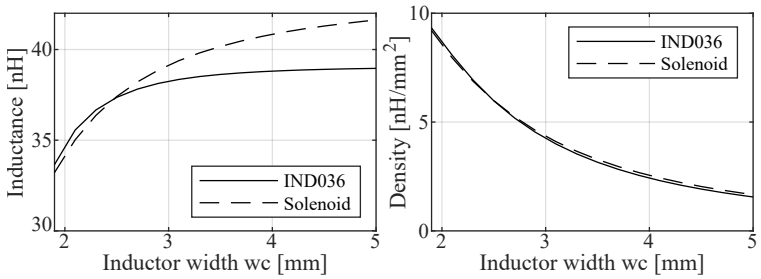


Figure 2.16: Inductance (left) and Inductance density (right) at 10 MHz of the simulated solenoid and IND036 as a function of the substrate width.

When the coupling is not required, the slots can be omitted and the vias can be drilled directly on the magnetic substrate. However, there are two requirements to avoid the use of slots: the material must be compatible with electroless copper deposition, as it is part of the fabrication process as will be described in Chapter 4, and the magnetic material must be non-conductive.

With this inductor design, several inductors can be fabricated in the same magnetic substrate for multiphase package IVR modules, increasing the level of power delivery granularity. The integration between the embedded inductors and the power stage circuitry, to form the package IVR, is shown in the cross-section in Figure 2.17.

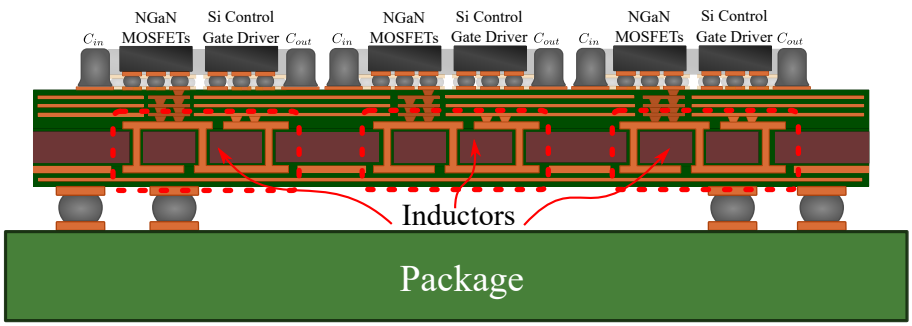


Figure 2.17: Multiphase package IVR integration

For a broader space of exploration, inductors can be optimized using machine learning techniques. In [55] and [56] it is shown how an artificial neural network (ANN) can be used to fine-tuning the inductor parameter for a given target function, which can be the inductor or system efficiency. However, these methods rely on a given structure and only change its parameters such as the number of turns, copper width and thickness, line space, magnetic

core thickness, etc., and they are not designed to find new and different structures. On the other hand, evolution or genetic algorithm have been successfully used to find new antenna structures [57, 58], where the algorithm adds wire elements to the 3D model to improve its performance. In [59] a genetic algorithm was demonstrated that, by evolution, it can design new RFID antenna structures.

2.4 Summary

Integrated inductors, as required for high voltage or high performance integrated voltage regulators, have been the major bottleneck for a high integration density. Surface mount inductors can be easier to fabricate, however, they take too much lateral space increasing considerably the required IVR space.

A common inductor like a solenoid, or any inductor with an open magnetic path, cannot be used as an embedded inductor. When an open magnetic path inductor is placed between conduction planes, its inductance and quality factor can be reduced by 35%. However, inductors with a closed magnetic path, like a toroidal inductor, can be embedded without affecting its performance.

In contrast to a discrete magnetic core, a large magnetic sheet substrate provides a close magnetic path for both types of inductors. The vias used to connect both sides of the magnetic substrate are responsible to build up the inductance. Using this concept, a large set of inductor structures were explored. With this novel design exploration, we arrived to an interleave incomplete toroidal inductor structure, which is simple to fabricate, has all the properties of a toroidal inductor and has several degrees of freedom for optimization.

In this structure, several vias are arranged in three or more slots drilled through a magnetic sheet substrate. The slots allow to couple the via's magnetic field and provide electrical isolation. The magnetic field is built around the central vias with an elongated toroidal field distribution, and the magnetic field is confined to the inductor structure even if the magnetic sheet is much larger. With a structure like this, it is possible to fabricate several

embedded inductors in the same substrate, as required for multi-phase buck converters. Several inductors were explored to determine the best design candidates and fabricate them for further experimental characterization.

CHAPTER 3

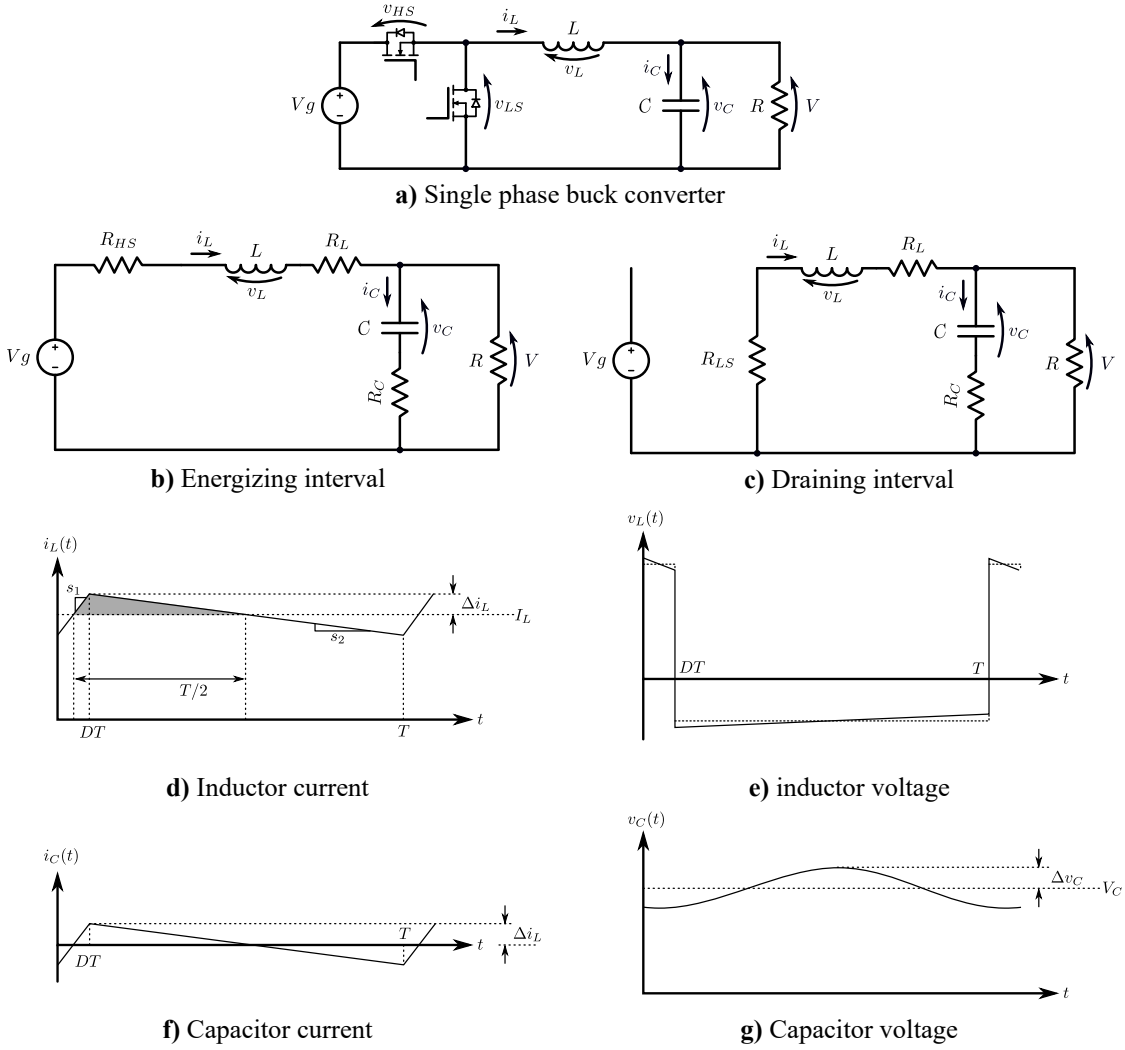
INDUCTOR CO-DESIGN AND POWER LOSS CALCULATION METHOD

For high conversion ratio IVRs, it is required a co-design between the power stage and the inductor. In this chapter, the buck converter design and power loss equations are presented. Accurate quantification of each component's losses is needed to determine the appropriate switching frequency, duty cycle, and inductance. Using these power loss expressions we derive a new metric called Effective AC resistance per unit inductance of R_{acx} which is then used as a method for the inductor power loss calculation.

3.1 Buck converter

In Figure 3.1(a) the basic single-phase buck converter is presented. The buck converter uses two MOSFETs: high side (HS) and low side (LS), one inductor, and one capacitor. The MOSFETs are driven by a circuit called gate driver which is not included in the drawing. This circuit topology operates in two states, as shown in Figure 3.1(b) first the HS switch is in *ON* state energizing the inductor during the time interval $0 < t < DT_S$, then as shown in Figure 3.1(c) the LS switch is in *ON* state draining the inductor energy to the load during the time $DT_s < t < T_S$.

During the steady state, the average inductor voltage must be zero, otherwise, the current would increase indefinitely. Similarly, the average capacitor current must also be zero. With these conditions, the circuit equations for inductor DC current I_L, inductor current ripple Δi_L, capacitor DC voltage V, and capacitor voltage ripple Δv_C can be obtained. For a detailed derivation of these results, the reader is referred to [6]. For the inductor analysis, what matters the most is the relation between duty cycle D, inductance L, and inductor



a) Single phase buck converter

b) Energizing interval

c) Draining interval

d) Inductor current

e) inductor voltage

f) Capacitor current

g) Capacitor voltage

Figure 3.1: Simple buck converter topology. (a) Single phase buck converter. (b) Energizing sub-interval. (c) Inductor draining sub-interval. (d) and (e) inductor waveforms. (f) and (g) capacitor waveforms.

current ripple Δi_L. The duty cycle D is given by

$$D = \frac{V + I_L(R_L + R_{LS})}{V_g - I_L(R_{HS} - R_{LS})} \cdot \frac{1}{\eta_e} \tag{3.1}$$

where η_e is a dynamic loss factor that will be introduced in section 3.4. The inductance for a given current ripple can be calculated as follow,

$$L = \frac{V_g - I(R_{HS} + R_L) - V}{2\Delta i_L} DT_S \approx \frac{V}{2\Delta i_L}(1 - D)T_s \tag{3.2}$$

and similarly, the current ripple for a given inductance can be calculated by,

$$\Delta i_L = \frac{V_g - I(R_{HS} + R_L) - V}{2L} DT_s \approx \frac{V}{2L}(1 - D)T_s \tag{3.3}$$

The filter capacitor C needs to be large enough so the output voltage ripple Δv_c stays in tolerance. The capacitor for a given output voltage ripple can be calculated as follow,

$$C = \frac{\Delta i_L}{8\Delta v_C} T_S \tag{3.4}$$

3.2 Passive Losses

As passive losses, we have the power loss due to the MOSFET on-resistance, the inductor copper resistance, and the magnetic conductivity and hysteresis. The losses due to the MOSFET and copper is given by,

$$P_{DC} = \left(I^2 + \frac{\Delta i_L^2}{3}\right)[DR_{Q1,on} + (1 - D)R_{Q2,on}] + I^2 R_{L,DC} + \frac{\Delta i_L^2}{3} R_C \tag{3.5}$$

The inductor RMS current is useful to calculate the losses in components that do not depend on the frequency, if that is not the case we need to obtain the frequency spectrum of the current using a Fourier series. Figure 3.2 shows the AC current waveform of the inductor.

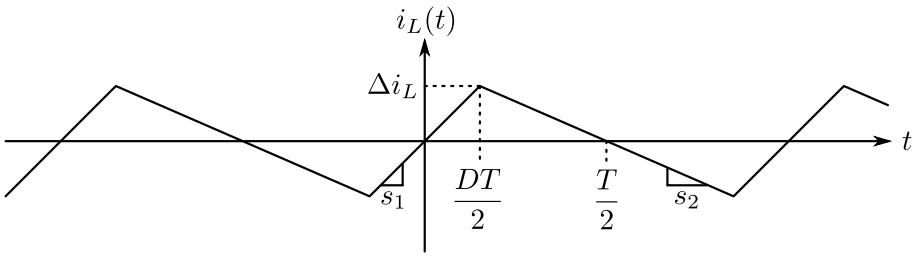


Figure 3.2: Inductor AC current waveform

This is a piece-wise function which formula is,

$$i_L(t) = \begin{cases} 2t\frac{\Delta i_L}{DT} & 0 < t \leq \frac{DT}{2} \\ \left(1 - \frac{2t}{T}\right)\frac{\Delta i_L}{1-D} & \frac{DT}{2} < t \leq T \end{cases}$$

Using a sine Fourier series expansion, it can be express as,

$$i_L(t) = \sum_{n=0}^{\infty} b_n \sin\left(\frac{2n\pi}{T}t\right)$$

where b_n is given by the next integral formula,

$$b_n = \frac{4}{T}\int_0^{T/2} i_L(t)\sin\left(\frac{2n\pi}{T}t\right)dt$$

which is evaluated to give the next result (for a detailed derivation see Appendix A),

$$b_n = \frac{2\Delta i_L}{D(1-D)}\frac{\sin(n\pi D)}{(n\pi)^2} \tag{3.6}$$

and the AC losses can be computed using the sine Fourier series expansion (for a detailed derivation see Appendix B), where $\omega_n = 2n\pi f_s$,

$$P_{AC} = \frac{1}{2}\sum_{n=1}^{N} b_n^2 \left[R_{L,ac}(\omega_n) + R_{L,core}(\omega_n)\right]$$

$$P_{AC} = \frac{2\Delta i_L^2}{D^2(1-D)^2}\sum_{n=1}^{N}\frac{\sin^2(n\pi D)}{(n\pi)^4}\left[R_{L,ac}(\omega_n) + R_{L,core}(\omega_n)\right] \tag{3.7}$$

where $R_{L,ac}$ are the losses due to copper resistance and eddy currents in the magnetic material, and $R_{L,core}$ are the hysteresis and excess losses. For the next development, we are going to consider only the small losses $R_{L,ac}$. Later, it will be demonstrated with measurements that this expression is also valid for $R_{L,core}$ at some conditions.

3.3 Dynamic Losses

Four types of dynamic losses for GaN MOSFETs are described in detail in [53] and summarized in Appendix C. These four loss mechanisms correspond to: Gate Charge Losses P_G, Turn-on and Turn-off Losses P_{IV}, Output Capacitance Losses P_{oss}, and Reverse Conduction Losses P_{SD}. The gate charge and output capacitance losses are the dominant ones in high voltage regulators, and are produced by parasitic capacitances between the MOSFET terminals. To understand these loss mechanisms, let consider the simple RC network shown in Figure 3.3.

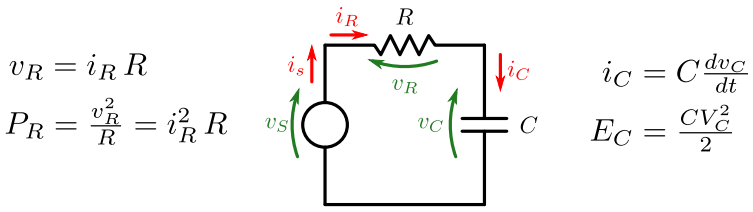


Figure 3.3: Simple RC network describing the loss mechanism.

A capacitor does not dissipate energy, however, depending on the way this capacitor is charged or discharged, the resistor R will dissipate more or less power. When the source is a constant current source, i.e. $i_s(t) = I_s$, the energy dissipated between $0 < t < T$ is,

$$E_R = I_s^2 RT \tag{3.8}$$

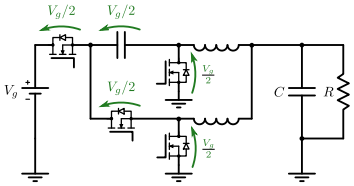
then the lower the R is, the lower the power loss. However, if the source is a constant voltage source, i.e. $v_s(t) = V_s$, then the energy lost in the resistor after the capacitor is fully charged is,

$$E_R = \frac{CV_s^2}{2} \tag{3.9}$$

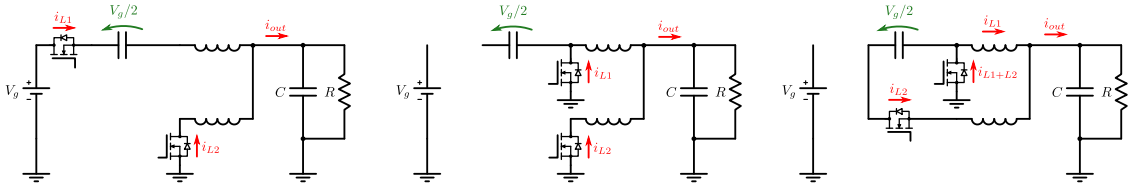
which is independent of R and the time taken to charge the capacitor. In such case, the power lost is

$$P_R = \frac{CV_s^2}{2} \cdot f_s \tag{3.10}$$

The power lost due to parasitic capacitance in a MOSFET increases linearly with frequency, and with the square of the voltage. Reducing the voltage over the MOSFET by half can reduce the output capacitance losses by a factor of four. A series capacitor buck converter [32] is a two or more phases buck converter topology that combines a switched capacitor with the inductors to reduce the voltage over the MOSFET by a factor k, where k is the number of phases. Figure 3.4 shows the circuit along with the three sub-interval states. During sub-interval 1, phase 1 is energized while phase 2 is draining. During sub-interval 2 both phases are draining. In sub-interval 3 the fly-capacitor energizes the phase 2 while phase 1 remains in draining mode. After sub-interval 3, the circuits go back to sub-interval 2. Then it starts again from sub-interval 1. This process has the result, in the steady state, that the flying capacitor gets charged with V_g/k, with $k = 2$ in this example. In consequence, phase 1 is powered by $V_g - V_C = V_g/2$, and phase 2 also by $V_C = V_g/2$. This reduction in phase voltage requires the duty cycle to be extended by the same factor k to obtain the same conversion ratio as the simple buck converter presented earlier.



a) Two-phase series capacitor buck converter



b) Sub-interval 1 c) Sub-interval 2 d) Sub-interval 3

Figure 3.4: Series capacitor buck converter topology. (a) Two-phases series capacitor buck converter. (b),(c),(d) circuit operation sub-intervals.

The number of phases can be incremented to further reduce the voltage over the MOSFETs. It must be noted that the duty cycle never can be greater than $1/k$, limiting the minimum conversion ratio. For example, with $V_g = 5$ V, $V = 1$ V, and 2 phases the duty

cycle should be approximately $D = 2 \cdot 1/5 = 0.4$, but in the voltage regulation control loop, the duty cycle never can be equal to $1/k = 1/2 = 0.5$, making it difficult to control. With $V_g = 12$ V instead, the duty cycle would be $D = 2 \cdot 1/12 = 0.167$. With $V_g = 48$ V and 4 phases, the duty cycle would be close to $D = 2 \cdot 1/48 = 0.083$. The expression for the duty cycle of a series capacitor buck converter is given by,

$$D_{sc} = \frac{kV + I\left(R_L + R_{LS}\right)}{V_g - I\left(R_{HS} + R_{fly} + \frac{R_{LS}}{2}\right)} \cdot \frac{1}{\eta_e} \tag{3.11}$$

3.4 Duty cycle dynamic factor η_e

The efficiency factor η_e is given by,

$$\begin{aligned} P_{XSW} &= P_{IV} + P_{SD} \\ \eta_e &= \frac{P_L + I_L V}{P_{XSW} + P_L + I_L V} \end{aligned} \tag{3.12}$$

where P_L is the inductor power loss and $I_L V$ is the power delivered to the load. This factor takes into account the MOSFET transfer losses P_{XSW} due to voltage-current overlap P_{IV} during transitions and the reverse conduction losses P_{SD}. When either MOSFET is turned on or off, both current and voltage across the MOSFET are non-zero during the transition resulting in a power loss P_{IV}. Similarly, when the high-side MOSFET Q_{HS} is turned off, there is a small fraction of time called dead-time or t_d where the body diode of the low-side MOSFET Q_{LS} conduct resulting in a power loss P_{SD}. By MOSFET transfer losses we refer to the power provided by the source that is meant to reach the load. Note that the output capacitance losses P_{oss} and gate charge losses P_g does not alter the duty cycle, since this power is meant to change the state of the MOSFET, not to reach the load. In Appendix D it is shown a power loss and duty cycle accuracy calculation example.

3.5 Inductor Power Loss Metric

In an inductor, there are several loss mechanisms, which are also a function of frequency. We can decompose the inductor power loss into three parts, as shown in (Equation 3.13): DC conduction losses $P_{L,DC}$, eddy current losses (in both copper and magnetic material) $P_{L,AC}$, and magnetic core losses $P_{L,H}$ (hysteresis and excess losses).

$$P_L = P_{L,DC} + P_{L,AC} + P_{L,H} \tag{3.13}$$

The hysteresis loss $P_{L,H}$ is given by the BH hysteresis loop where the density of energy lost per switching cycle is $U = \int H \cdot dB$ [J m^{-3}]. The power loss is found by multiplying U by the effective inductor volume and switching frequency. However, as shown in [8] and [7], the hysteresis losses are also affected by the duty cycle D. Several methods, including the Steinmetz Equation (SE), Modified SE, and Generalized SE, have been used to model the inductor core losses when non-sinusoidal excitations are applied. These models require to know the magnetic flux B, however, the value of B is non-uniform inside the inductor and therefore difficult to quantify. In this thesis, we study the relation of more circuit friendly quantities, such as inductance L and inductor current ripple Δi_L, to model and understand the inductor losses with non-sinusoidal currents. We start by deriving an expression to quantify the small signal losses $P_{L,DC}$ and $P_{L,AC}$, to then compare it with the large signal losses P_L.

The DC and AC power losses are

$$P_{L,DC} = I_L^2 R_{DC} \tag{3.14}$$

$$P_{L,AC} = \frac{2\Delta i_L^2}{D^2(1-D)^2} \sum_{n=1}^{N} \frac{\sin^2(n\pi D)}{(n\pi)^4} R_{AC}\left(\frac{n}{T_s}\right) \tag{3.15}$$

where $P_{L,AC}$ is derived in detail in Appendix B.

From the AC power loss expression, we observed we can factor out the inductor current

ripple Δi_L^2. We know that the dimension of energy is $Joule = Amperes^2 \times Henry$. Then we can transform the expression to have the form $\Delta_L^2 L r_{acx}$, where the variable $r_{acx}(D, f_s)$ is defined here as the small signal effective AC resistance per unit inductance with units of $\Omega\,\mathrm{H}^{-1} = s^{-1}$, and is given as follows,

$$r_{acx} = \frac{2}{D^2(1-D)^2} \sum_{n=1}^{N} \frac{\sin^2(n\pi D)}{(n\pi)^4} \frac{R_{AC}(nf_s)}{L(f_s)} \tag{3.16}$$

We can now combine equations (Equation 3.14), (Equation 3.15), and (Equation 3.16) to obtain the next inductor power loss expression,

$$P_L = I_L^2 R_{DC} + \Delta i_L^2\, L(f_s)\, r_{acx}(D, f_s) + P_{L,H} \tag{3.17}$$

Since the expression $\Delta i_L^2\, L(f_s)$ has units of Joule, r_{acx} correspond to an energy loss rate factor and is a measure proportional to how much energy, due to the AC current, is lost per cycle. Using the inductor presented in the following sections, it will be shown that r_{acx}, for both small and large signal, is indeed independent of the amount of inductance and current ripple. In addition, it will be shown with measurements that the large signal power loss $P_{L,H}$ has some relation to r_{acx} and we can write the total power loss as follows,

$$P_L = I_L^2 R_{DC} + \Delta i_L^2\, L(f_s)\, \kappa(f_s)\, r_{acx}(D, f_s) \tag{3.18}$$

where κ is the large to small signal ratio and, below some frequency, it is independent of the duty cycle and current ripple. For the total AC losses we have $R_{acx} = \kappa r_{acx}$.

3.6 Inductor Requirements

Every switching cycle the inductor is charged with additional energy ΔE_L, which is then transfer to the load. This amount of energy is given by (Equation 3.19), provided the in-

ductor is not saturated and the inductance remains constant over the integration limits.

$$\Delta E_L = \int_{i_L(0)}^{i_L(DT_s)} L\, i_L di_L = 2LI_L\Delta i_L = I_L V(1-D)T_s \tag{3.19}$$

The inductor power loss expression can be rewritten using the delta energy (Equation 3.19) as follows,

$$P_L = I_L V\alpha + 2L(f_s)I_L\Delta i_L f_s\,\beta \tag{3.20}$$

where α is the DC loss factor due to the parasitic DC resistance, and β is the inductor AC loss factor and tells how much of the energy stored in the inductor is lost when it is released to the load. Both factors are unit-less. The variables α and β are defined as

$$\alpha = \frac{I_L}{V}\,R_{DC} \tag{3.21}$$

$$\beta = \frac{\Delta i_L}{2I_L f_s}\,R_{acx} \tag{3.22}$$

As will be shown later, with 0 A of DC current, R_{acx} can be given by $R_{acx} = P_L/\Delta i_L^2 L$, and therefore is not limited to the small signal losses, but to the total inductor AC losses. From (Equation 3.19) we note that $2LI_L\Delta i_L f_s = I_L V(1-D)$, then we can simplify the power loss (Equation 3.20) as follow,

$$P_L = I_L V\left(\alpha + (1-D)\beta\right) \tag{3.23}$$

The inductor efficiency η_L is defined as the ratio of the power delivered to the load over the power delivered to the inductor:

$$\eta_L = \frac{I_L V}{I_L V + P_L} = \frac{1}{1+\alpha+(1-D)\beta} \tag{3.24}$$

The power-related equivalent series resistance R_L of the inductor is defined by,

$$R_L = \frac{P_L}{I_{L,RMS}^2} = \frac{I_L V}{I_{L,RMS}^2}(\alpha + (1-D)\beta) \tag{3.25}$$

It is difficult to make a sensitivity analysis of the efficiency with respect to the duty cycle and frequency. The inductor efficiency and duty cycle can only be obtained recursively since the D depends on R_L which in turn depends on η_L, where again η_L depends on D. However, in the big picture, we can observe that even though the inductor losses will be maximum with a duty cycle close to 1 (or close to 0 as will be shown later with measurements of r_{acx}), with $D = 1$ the efficiency will be maximum and equal to,

$$\eta_{max} \underset{D\to 1}{=} \frac{1}{1+\alpha} \tag{3.26}$$

and therefore, the inductor efficiency will always increase with longer duty cycles.

With respect to frequency is more complicated because the inductor efficiency depends on the actual loss profile of the magnetic materials. With higher frequencies, the inductor efficiency can be higher or lower and will depend whether Δi_L^2 decrease faster than the increase of R_{acx}, or not.

Buck converters, or voltage regulators in general, are designed for a maximum output power or current. In Figure 3.5 it is shown that there is a single maximum for the efficiency with respect to current, and the design must be done such that this maximum occurs at the most common output value, which is usually designed as 75% of the maximum output current.

During design, the maximum inductor should also coincide with the maximum MOSFET or power stage topology efficiency point. Let's denote I_M as the output DC current at maximum inductor efficiency, then the inductor power loss at maximum efficiency is given by,

$$P_L = I_M\, V \left(\frac{1}{\eta_L} - 1\right) \tag{3.27}$$

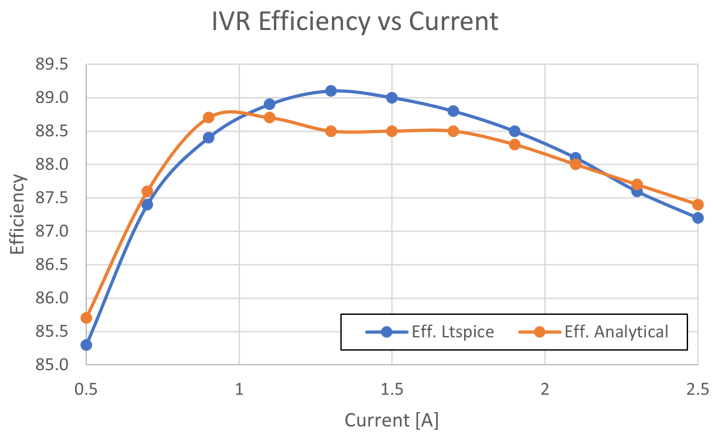


Figure 3.5: Typical efficiency versus current of a voltage regulator.

From the inductor efficiency (Equation 3.24), to maximize the efficiency with respect to the load current I_M we need to minimize the expression $\alpha + (1-D)\beta$. From the definition of α and β we have,

$$\begin{aligned}\frac{d}{dI_M}\left\{\frac{I_M\,R_{DC}}{V} + (1-D)\frac{\Delta i_L}{2I_M\,f_s}R_{acx}\right\} &= 0\\ = \frac{R_{DC}}{V} - (1-D)\frac{\Delta i_L}{2I_M^2,f_s}R_{acx} &= 0\\ = \alpha - (1-D)\beta &= 0\end{aligned}$$

this result means that, to obtain the maximum efficiency for a given output DC current I_M, the DC and AC losses must be equal, hence $\alpha = (1-D)\beta$.

The (Equation 3.18) is rewritten by replacing the current ripple using (Equation 3.3),

$$P_L = I_M^2 R_{DC} + \frac{V^2}{4Lf_s^2}(1-D)^2\,R_{acx} \tag{3.28}$$

then R_{DC} is obtained by:

$$R_{DC} = \frac{P_L}{2}\frac{1}{I_M^2} \tag{3.29}$$

this sets the upper bound for the DC resistance. Naturally, any lower value will yield lower

losses. For the AC loss $P_{L,AC}$ we obtain the next condition:

$$\frac{V^2(1-D)^2}{4Lf_s^2}R_{acx} = \frac{P_L}{2} \tag{3.30}$$

The two inductor parameters from the previous equations are L and R_{acx}. The duty cycle D and switching frequency f_s are set by the application conversion ratio which is decided as design choices. Therefore, the previous expression can be written as:

$$\frac{\widetilde{R}_{acx}}{L} = \frac{P_L}{2}\frac{4f_s^2}{V^2(1-D)^2} = M\left[\frac{\Omega}{\mathrm{H}^2}\right] \tag{3.31}$$

where $\widetilde{R}_{acx}$ is the maximum required value, not the measured one. Higher values of $\widetilde{R}_{acx}$ allows for less efficient magnetic materials, since the measured R_{acx} needs to be lower than $\widetilde{R}_{acx}$. The inductance L and the resistance per unit inductance $\widetilde{R}_{acx}$ are related by the constant $M > 0$. Since the $\widetilde{R}_{acx}$ and its relation to L has an inverse quadratic dependence on $1 - D$, an accurate value for the duty cycle is required.

Also, we can observe from (Equation 3.31) that the lower the duty cycle is, the higher will be the required inductance and the lower the required $\widetilde{R}_{acx}$. Basically, lower duty cycle means making more use of the inductor and as result, it will produce more losses. In the limits, if $D \to 1$ then even for very low inductances the $\widetilde{R}_{acx} \to \infty$. This make sense because with $D = 1$ we don't need any inductor at all. However, if $D \to 0$, then L will be maximum and $\widetilde{R}_{acx}$ will be minimum with respect to D.

With accurate values of the duty cycle D, we can obtain the $\widetilde{R}_{acx}$ to inductance L ratio. Figure 3.6 and Figure 3.7 show the values of $\widetilde{R}_{acx}$ and Δi_L versus inductance required for conversion ratios of 48 V to 1 V and 12 V to 1 V at different frequencies. From these figures, we can extract the required inductor properties which are summarized in Table 3.1.

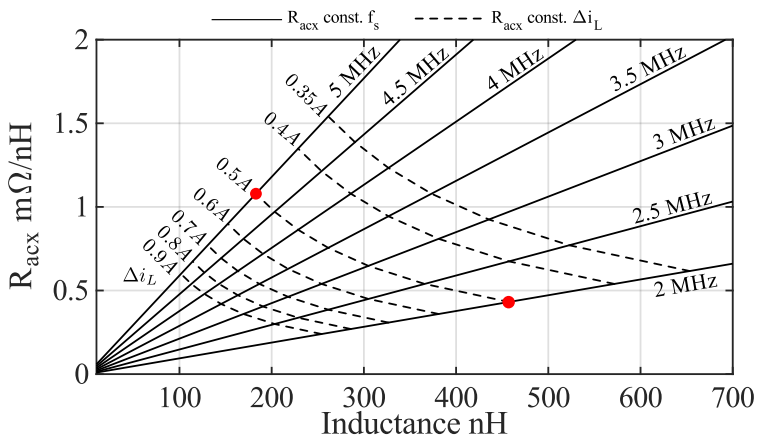


Figure 3.6: $\widetilde{R}_{acx}$ vs L for $V_g = 48$ V, $D = 0.0925$, $R_{DC} = 14$ mΩ. The dash lines correspond to constant current ripple Δi_L points.

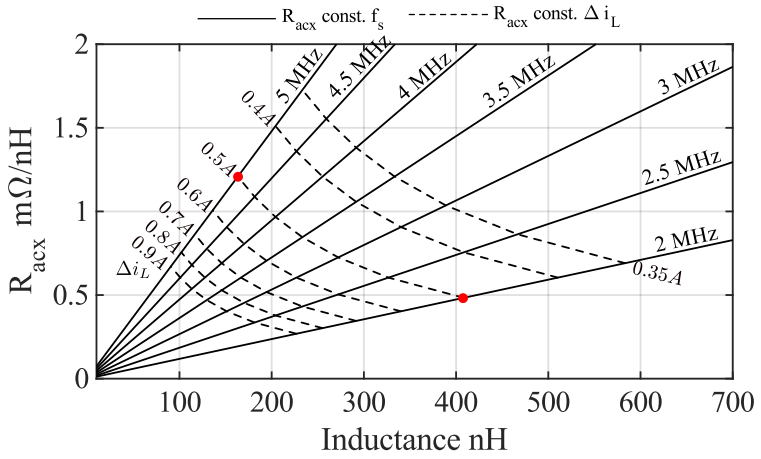


Figure 3.7: $\widetilde{R}_{acx}$ vs L for $V_g = 12$ V, $D = 0.1834$, $R_{DC} = 14$ mΩ. The dash lines correspond to constant current ripple Δi_L points.

Table 3.1: Inductor requirements with $\Delta i_L = 0.5$ A and , $R_{DC} = 14$ mΩ.

V_g	D	f_s MHz	L nH	$\widetilde{R}_{acx}$ mΩ/nH
48	0.0925	5.0	183	1.079
48	0.0925	2.0	457	0.432
12	0.1834	5.0	163	1.208
12	0.1834	2.0	408	0.482

In comparison, Figure 3.8 shows the required $\widetilde{R}_{acx}$ and inductance L for 1.7 V to 1 V conversion ratio. At 5 MHz, this conversion ratio only requires 70 nH with $\widetilde{R}_{acx} = 2.8$ mΩ/nH. For high conversion ratio, more than twice the inductance with less than half $\widetilde{R}_{acx}$ are required. This shows how challenging the task of 48 V to 1 V and 12 V to 1 V is

compared to low voltage and low conversion ratio voltage regulator.

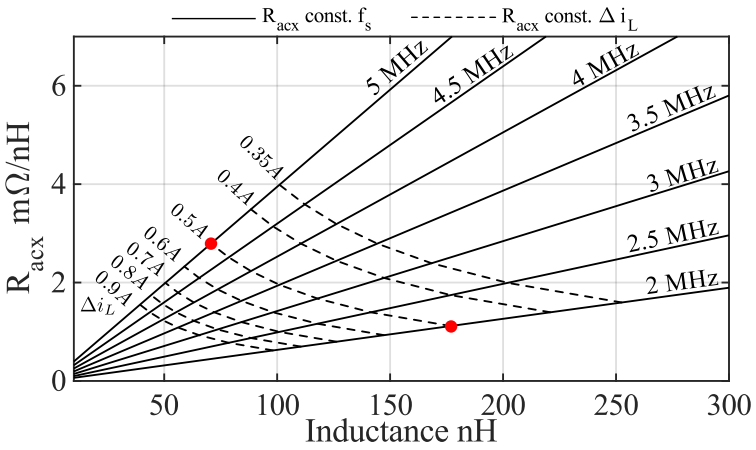


Figure 3.8: $\widetilde{R}_{acx}$ for $V_g = 1.7$ V, $D = 0.646$, $R_{DC} = 14$ mΩ.

We can start to analyze and optimize the inductors, shown in the previous section, to meet the target values of inductance, DC resistance, and R_{acx}. This will be done in the next Chapter where the available magnetic materials are presented.

3.7 Inductor Measurement Methods

But before we can design and fabricate the inductors, we need to know how to measure them so we can validate the ideas presented in this section. We need several types of measurements to do so. A small signal measurement, where the inductor is excited with a low power signal, is used to obtain the inductance and AC resistance profile as required to calculate the r_{acx}. The same small signal measurement needs to be obtained with a DC bias current to know the maximum current the magnetic material support before it saturates. Finally, a large signal measurement, where the inductor is excited with a large non-sinusoidal current, is required to find the factor κ and the total inductor losses.

The three described measurements require different setups. It is difficult to use a single probing structure for all the measurements, because of structure will introduce additional errors. For the small signal setup we can use Groud-Signal-Ground (GSG) RF probes to minimize the error, but depending on the frequency range the inductor is connected

in different ways. For the DC bias setup, the RF probes cannot handle more than a few amperes of current, therefore, different probing points would be required. Finally, for the large signal measurement the inductor needs to be mounted in a buck converter in a PCB, and so, RF probing point cannot be used.

In this work, 7 different inductor designs with 6 different materials are fabricated. It would become too expensive and time-consuming to fabricate the 42 inductors with all the different probing structures. That would require fabricating over 168 different inductors. To solve this, a single probing structure with a two-level calibration will be used. The second calibration is used for device de-embedding.

3.7.1 Small Signal Measurement with De-embedding

To cover a broad frequency range from 100 kHz to 1 GHz, two measurement setups as shown in Figure 3.9 are needed. Below 100 MHz a shunt-thru method is used because the inductor impedance below 10 MHz is lower than 50 Ω. Above 10 MHz a series-thru method is used as the inductor impedance above 100 MHz is greater than 50 Ω. As sanity-check, both methods must give the same result between 10 MHz and 100 MHz. In addition, a 2-level calibration is needed. A SOLT (Short, Open, Load, Thru) calibration is performed at the end of the VNA SMA connection ports 1 and 2, and an SOL (Short, Open, Load) calibration structure (fabricated in the same samples of the second inductor batch) is used to find the Error Box shown in Figure 3.9.

For the error box, considering the impedance model shown in Figure 3.10, we can write the next equations for the three calibration standards $Z_{M|open}$, $Z_{M|short}$, $Z_{M|load}$,

$$Z_{M|open} = Z_1 + Z_2 \tag{3.32}$$

$$Z_{M|short} = Z_1 + \frac{Z_2\, Z_3}{Z_2 + Z_3} \tag{3.33}$$

$$Z_{M|load} = Z_1 + \frac{Z_2(Z_e + 50)}{Z_2 + Z_3 + 50} \tag{3.34}$$

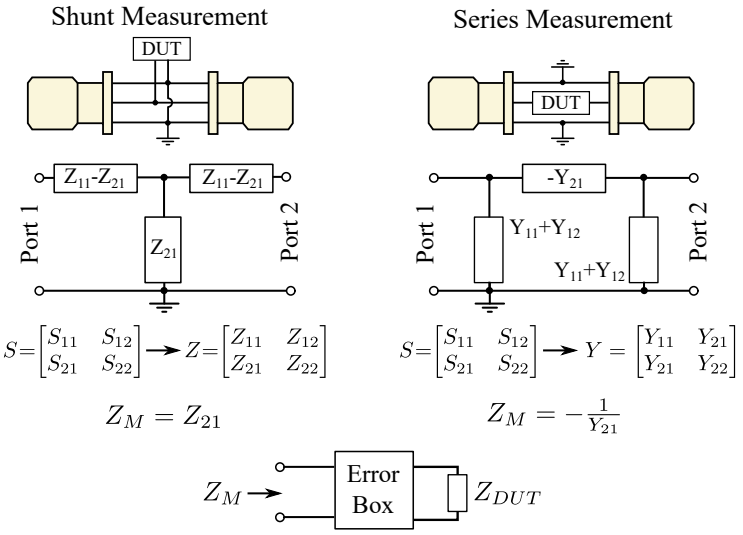


Figure 3.9: Inductance model for shunt S parameters measurement.

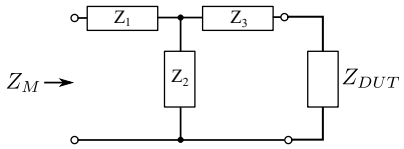


Figure 3.10: Impedance model for error box.

These three equations can be reduced to two writing them them in matrix form given a two-dimensional non-linear equation,

$$F(Z_2, Z_3) = \begin{bmatrix} Z_{M|open} - Z_2 + \frac{Z_2 Z_3}{Z_2+Z_3} - Z_{M|short} \\ Z_{M|open} - Z_2 + \frac{Z_2(Z_e+50)}{Z_2+Z_3+50} - Z_{M|load} \end{bmatrix} = 0 \tag{3.35}$$

then, solving for Z_1, Z_2, and Z_3 at each frequency point the DUT impedance Z_{DUT} can be extracted. The next equation is used to extract the DUT values, and Figure 3.11 shows an example of measured standard and then their extraction using the error box.

$$Z_{DUT} = \frac{Z_2 Z_3 + Z_1 Z_2 + Z_1 Z_3 - Z_M Z_2 - Z_M Z_3}{Z_M - Z_1 - Z_2} \tag{3.36}$$

Figure 3.12 shows the result of de-embedding a discrete toroidal inductor fabricated with HBS1 material. The error box effectively removes the errors introduced by the test

fixture, especially at higher frequencies.

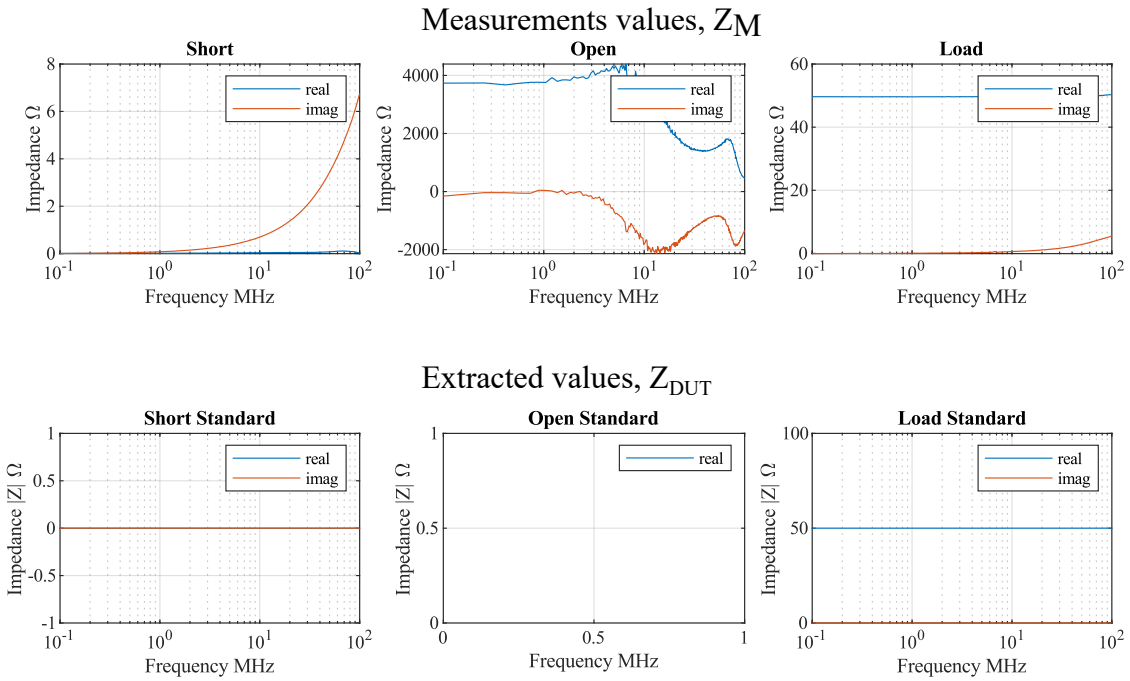


Figure 3.11: Measurement and extracted values for SOL standards.

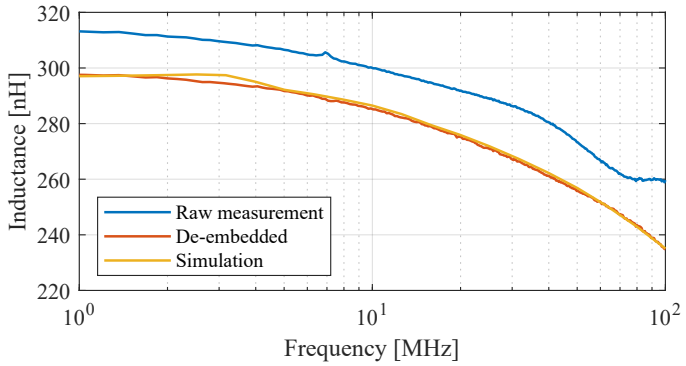


Figure 3.12: Measurement example for a discrete toroid with HBS1 material.

3.7.2 Small Signal with DC Bias

Figure 3.13 shows the measurement setup for the small-signal with DC bias current, where an isolated current source from Siglent™ model SPD3303X-E applies a bias current to the inductor. Two filter inductors of 6.8 μH with FRM (Ferromagnetic Resonance) of 18 MHz and saturation current of 5.5 A are used to provide a much larger impedance seen

towards the current source in comparison to the inductor to be measured. The inductor DC resistance is much smaller than the instrument. An SOL calibration is used to find the error box and remove the effect of the bias setup in the inductor measurement. Only a shunt-thru measurement is performed in the range of 100 kHz to 100 MHz.

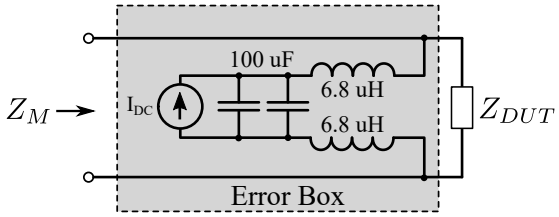


Figure 3.13: Small signal DC bias setup.

3.7.3 Large Signal

The large signal measurement setup is shown in Figure 3.14. For the large signal measurements, a dual isolated power supply from Siglent™ model SPD3303X-E was used to power the board and the MOSFETs. A signal generator from Siglent™ model SDG2042X was used to generate the MOSFET switching signal and oscilloscope trigger. An oscilloscope from Siglent™ model SDS1202X-E with 1 Gsps was used to record the inductor waveform.

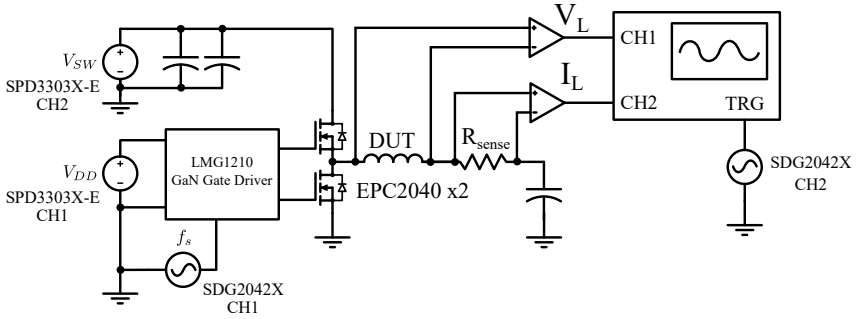


Figure 3.14: Large signal measurement setup.

The inductor waveform is obtained by a pair of 400 MHz bandwidth differential amplifiers. Figure 3.15 shows an example of recorded waveforms for the inductor voltage and current. The multiplication of these two gives the instantaneous power. The inductance is

calculated as,

$$L = \frac{v_L \Delta t}{\Delta i} \tag{3.37}$$

and the current ripple is just the half peak-to-peak current. The inductor power loss is obtained with the average of the inductor power waveform.

$$P_L = \frac{1}{t_1 - t_0} \int_{t_0}^{t_1} v_L(t) i_L(t)\, dt \tag{3.38}$$

Finally, the measured large signal R_{acx} is simply,

$$R_{acx} = \frac{P_L}{\Delta i_L^2 L} \tag{3.39}$$

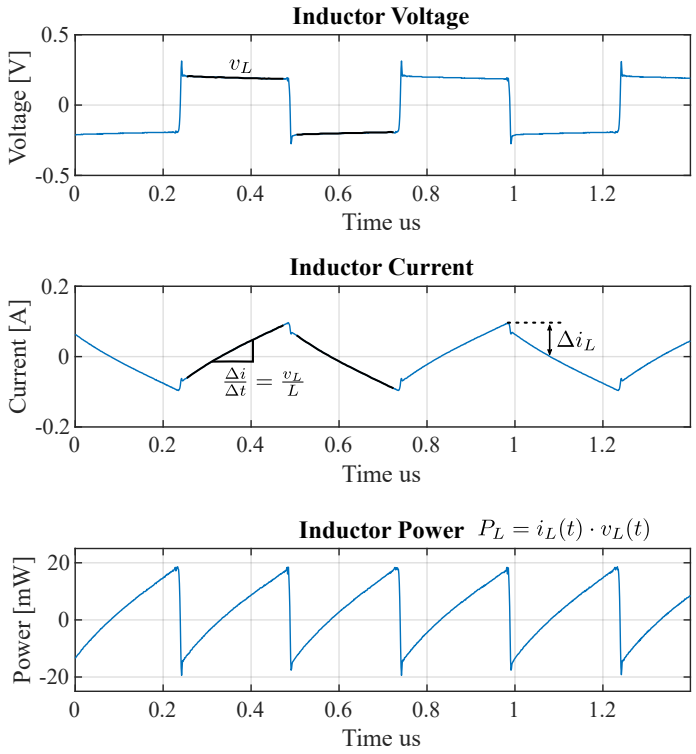


Figure 3.15: Inductor waveforms.

With the split power supply, we can easily differentiate between the power consumed by the gate driver and other circuits, and the power consumed by the MOSFETs (output capacitance, on-resistance, reverse conduction) and the inductor. A sanity-check includes

to verify the average inductor power loss calculated with the waveforms is always less than the measured power delivered by the power supply V_{SW}.

In the next chapter, it is shown the fabrication of six embedded inductor structures. With these inductors we compared the indirect measurement of r_{acx} (using the small signal inductance and resistance spectra) with the direct measurement of R_{acx} (using the large signal response).

3.8 Measurement Board

A test board for measurements was designed and fabricated. The board allows to measure the small signal with and without DC bias current using a VNA, and the large signal response using a buck converter with GaN MOSFET with independent control of input voltage, frequency, and duty cycle. Figure 3.16 shows the measurement board. To measure the DC resistance a 4-wire method and multimeter from Hewlett Packard™ model 34401A was used. To measure in the range of 10 MHz and 1 GHz, a VNA from Agilent Technologies™ model E8363B was used, and in the range of 100 kHz to 100 MHz an open source low frequency VNA, called nanoVNA V1, was used.

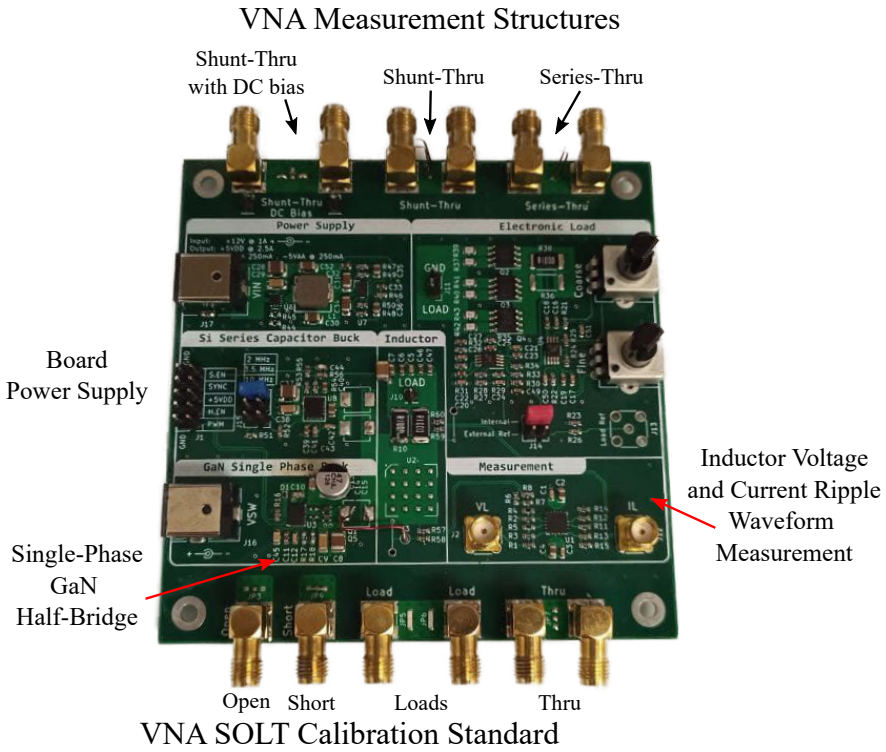


Figure 3.16: Measurement Board.

3.9 Summary

An accurate model to predict the system losses is fundamental to evaluate each component of the IVR, to determine the correct duty cycle used to analyze the performance of the inductor, and determine which components are those that contribute the most to the power loss. There are two types of losses: passive and active. The passive losses are those that produce para parasitic resistance on the components including the MOSFETs channel on-resistance and inductor resistance. The active losses are produced every time a MOSFET transitions between ON and OFF states. Some of these losses will have an impact on the duty cycle and so they must be taken into account.

In particular, the inductor losses can be divided into the DC conduction losses $P_{L,DC}$ produced by the DC resistance, eddy current losses (in both copper and magnetic material) $P_{L,AC}$, and magnetic core losses $P_{L,H}$ (hysteresis and excess losses). The $P_{L,AC}$ losses are also known as the small-signal losses and the $P_{L,H}$ as the large-signal losses. A new metric

called Effective AC resistance per unit inductance, or R_{acx}, is presented and used to easily determine the small-signal losses including the effect of the duty cycle and frequency. It is also presented a set of equations used to determine the inductor properties, such as DC resistance R_{DC}, Inductance L, and R_{acx}, for a given conversion ratio, frequency, and target inductor efficiency. The properties for 48 V to 1V and 12 V to 1 V conversion ratio are used to guide the inductor designs presented in this thesis. The fabricated inductors are analyzed with this metric, where additional properties for the R_{acx} values are obtained. This study shows the next requirements: DC resistance of 14 mΩ, inductance greater than 400 nH and 2 MHz and greater than 160 nH at 5 MHz, and a R_{acx} of less than 1.5 mΩ/nH.

In this section, the measurement methods and setups were explained. A dedicated board was designed and fabricated to perform the three basic measurements: small signal, small signal with DC current superposition, and large signal response. A 2-level calibration method was described, which is used to de-embedded the DUT from measurements. Finally, a method to directly measure the large signal R_{acx} was presented. The large signal R_{acx} will be compared to the small signal r_{acx} extracted from the small signal inductance and resistance spectra, to show the relation and that (Equation 3.7) is indeed valid.

To validate all these new ideas we need to make accurate measurements of several types. In this work, 7 different inductor designs with 6 different materials are fabricated. It would become too expensive and time-consuming to fabricate the 42 inductors with all the different probing structures. That would require fabricating 168 different inductors. To solve this, a single probing structure with a two-level calibration is used.

CHAPTER 4

MAGNETIC MATERIAL AND FABRICATION PROCESS

IVRs require highly integrated components, including power MOSFET and inductors. Embedding of passives components is key to obtain smaller solutions allowing them to be closer to the integrated circuits (IC), thus reducing the interconnection lengths, associated parasitics, and improving power density. In particular, inductor embedding has been limiting the miniaturization and performance of IVRs [60]. This has been attributed to the limited performance of the commonly used magnetic materials such as ferrites and nanocomposite thin-films with respect to the permeability, thickness, frequency stability, and loss properties of the materials. These factors affect the inductance and current density of the inductors. So far, an optimal trade-off between these performance parameters has been primarily achieved by surface-mount inductors.

To overcome the challenges of magnetic materials at high frequency for high power embedded applications, different air-core package embedded inductors were shown in [22]. However, these implementations can only achieve inductances in the range of 1 to 7 nH, with DC resistance in the range of 6 to 36 mΩ. Other magnetic thin-film technologies as presented in [14] can achieve higher inductances close to 20 nH but still with high DC resistance of 92 mΩ. Even though these technologies can achieve very high inductance density, they cannot be scaled to obtain 100's of nH with DC resistances lower than 20 mΩ as required for single stage 48V to 1V and 12V to 1V converter.

Recently, there has been a shift towards newer classes of materials such as metal-powders and metal-polymer composites (MPC) for inductor cores [61, 62]. In these materials, metal fillers coated with an insulating metal-oxide layer are embedded in epoxy polymers. The epoxy behaves as a distributed air gap reducing the core hysteresis losses and increasing the saturation magnetic field, while the small coated particle reduces the

eddy current losses. It is also observed that the frequency stability improves. In [63] a comparison between metal-flakes composite and ferrite material is presented, where the composite solutions offer higher permeability with higher frequency stability, higher saturation current, and lower size. In this thesis, we leverage the advancement in composite magnetic materials in the form of magnetic sheets to develop a new process to fabricate the novel inductor structures presented previously.

Usually, inductors are designed to achieve a target amount of inductance and Q factor, most of the time, based on small signal measurements. However, as we show in this chapter, the large signal losses can be easily 5 times larger than the small ones, rendering any calculation base on small signal spectra invalid. But it is also true that it is very difficult to design an inductor with no clue how will the large signal behaves. Follow a trial and error on very complex devices, when the fabrication time is long and very expensive, should be avoided. In this work, we have proposed the metric effective AC resistance per unit inductance as a means to predict the small signal losses using the measured inductance and resistance spectra. Through measurements, we show that this metric is very insensitive to inductance and geometrical changes. This metric is then, also through measurements, compared to the large signal losses to found that the small to large signal losses can be easily related by a factor κ.

4.1 Review of Magnetic Properties

Considering the drawback of ferrites and nanocomposite thin films as discussed earlier, the favorable class of materials for power inductors are the Metal-Polymer Composites (MPC). The desired material properties are: 1) high permeability, 2) high saturation magnetization, 3) high-frequency stability, and 4) low loss tangent.

The permeability of particles in an MPC is different along different directions due to anisotropic shape [64]. If the magnetizing field $\vec{M}$ lies along with one of the principal axis of an ellipsoidal particle, the demagnetizing field $\vec{H}_M$ is given by $\vec{H}_M = -N\vec{M}$ with N

being the demagnetizing factor. The value of N depends on the principal ellipsoid axis (a,b, or c) the field is directed and it must obey the relation,

$$N_a + N_b + N_c = 1$$

It can be identified three cases: Prolate spheroid (long rod), Oblate spheroid (disc or flake), and Sphere. Figure 4.1 shows the values of N for the three cases. Depending on the inductor structure it can be preferable one to another composite filler or core shape. It must be noted that the anisotropic shape factor does not depend on the specimen size.

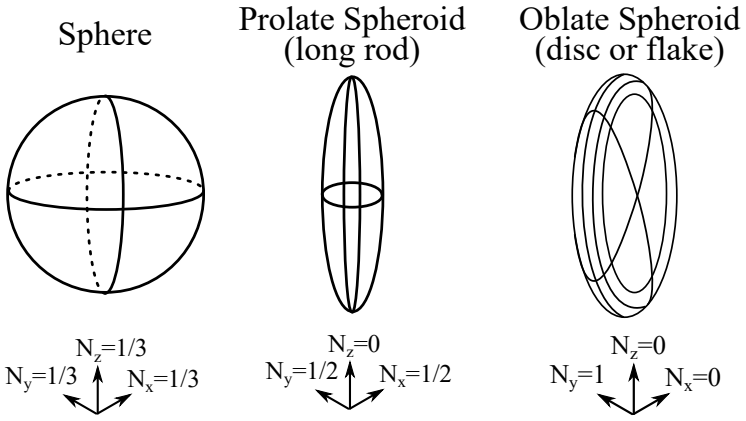


Figure 4.1: Shape factor for different types of filler.

In composite materials, the effective permeability can be first approximated using (Equation 4.1) [61], where p is the volume loading factor, N_0 is the demagnetization shape factor of magnetic fillers, and μ_i is the permeability of the magnetic fillers.

$$\mu_e = 1 + \frac{p}{N_0(1-p) + 1/(\mu_i - 1)} \tag{4.1}$$

therefore by increasing the loading factor and choosing the right filler shape the permeability can be increase. In MPC the effective relative permeability will be smaller than to its bulk counterpart due to volume loading ratio and shape anisotropy [65].

The permeability spectra can be modeled using the Lorentz and Landau-Lifshitz-Gilbert

equation shown in [61]. The equation is given by

$$\mu_e = 1 + \frac{\omega_d^2 \chi_{d0}}{\omega_d^2 - \omega^2 + j\beta\omega} + \frac{(\omega_s + j\alpha\omega)\omega_s \chi_{s0}}{(\omega_s + j\alpha\omega)^2 - \omega^2} \tag{4.2}$$

where χ_{d0} and χ_{s0} are the domain wall and spin magnetic susceptibilities, ω_d and ω_s are the resonant frequencies of each magnetic contribution, α, β are damping factors.

Since the permeability spectra is a complex value, it accounts for the inductance and the eddy currents losses in the magnetic material and windings. The core or hysteresis losses need to be calculated from the BH curve for the magnetic material. Therefore, a low coercivity is required for low hysteresis losses, and using a proper filler size in nanocomposite material is key since it has a direct impact on the coercivity $\vec{H}_c$ [66] and eddy current losses.

The ferromagnetic resonance limits the frequency stability of the inductor and is related to the shape factor, permeability, and magnetic saturation and there is a trade-off between permeability and ferromagnetic resonance where a high value for both cannot be obtained at the same time, this is called the Snoek's limit [62]. The FMR is defined by the Kittel expression as is shown in (Equation 4.3) [65].

$$f_{FMR} = \frac{\mu_0}{2\pi}\gamma\sqrt{[H_k + (A_x - A_z)M_s][H_k + (A_y - A_z)M_s]} \tag{4.3}$$

where M_s is the maximum attainable magnetization, H_k is the applied magnetic field, γ is the gyromagnetic ratio and is equal to 1.760859×10^{11} rad s^{-1} T^{-1}, and $\vec{A}$ is a demagnetizing factor that depends on the shape factor and volume loading fraction. For metal composite material with very low volume fraction $\vec{A} \approx \vec{N}$, and for a very high volume fraction (bulk limit) $\vec{A} \approx 0$.

For thin films or large magnetic sheets where large anisotropy is introduced, (Equation 4.3)

is reduced to (Equation 4.4) [62],

$$f_{FMR} = \frac{\mu_0 \gamma}{2\pi} \sqrt{H_k (H_k + M_s)} = \frac{\mu_0 \gamma}{2\pi} \frac{M_s}{\mu_r - 1} \sqrt{\frac{H_k + M_s}{H_k}} \tag{4.4}$$

Reduce the particle size and volume loading ratio can also help to increase the FMR since the polymer acts as a distributed air-gap that increases H_k. Regarding the eddy current losses, smaller particles exhibit lower induced current and therefore lower losses. However, when the volume loading is increased, particles start to touch each other increasing the effective particle size. To prevent this last issue particles can be coated with an oxide layer.

4.2 Magnetic Sheets

Five magnetic sheets, courtesy of Panasonic, named HPE1, HPE2, HBS1, MUE1, and MUF1 were used. In addition, the commercially available magnetic sheet from Kemet part number RM4A was used for comparison. These materials are separated into two categories: i) low frequency, high permeability, low saturation, and with flake fillers: HPE1, HPE2, and RM4A, and ii) high frequency, low permeability, high saturation, and with spherical fillers HBS1, MUE1, MUF1. Figure 4.2 shows the permeability and loss tangent spectra for these materials.

Magnetic materials are highly non-linear with respect to frequency and magnetic flux. The latter is characterized by the magnetic field intensity H created by the circulating current and the material intrinsic magnetic field B_i, with $B = \mu_0 H + B_i$. The Bi-H characteristic curve for the material HPE1, HPE2, RM4A, and HBS1 are shown in Figure 4.3. In the Figures, the blue lines correspond to the measured values, and the orange lines in the first quadrant were the ones used for saturation current simulation.

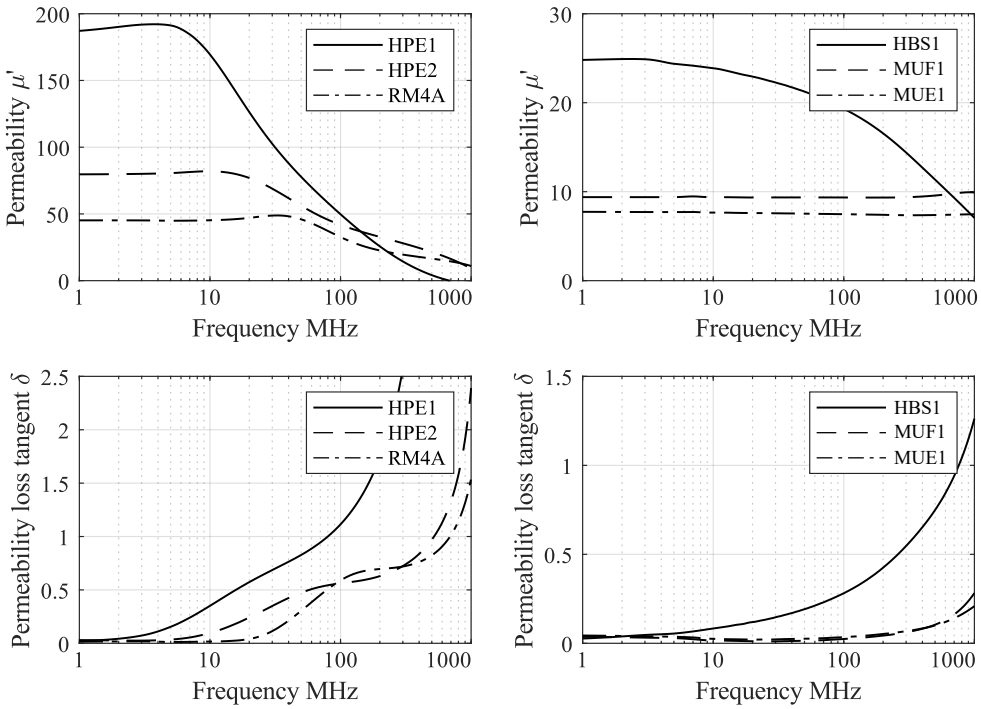


Figure 4.2: Permeability spectra.

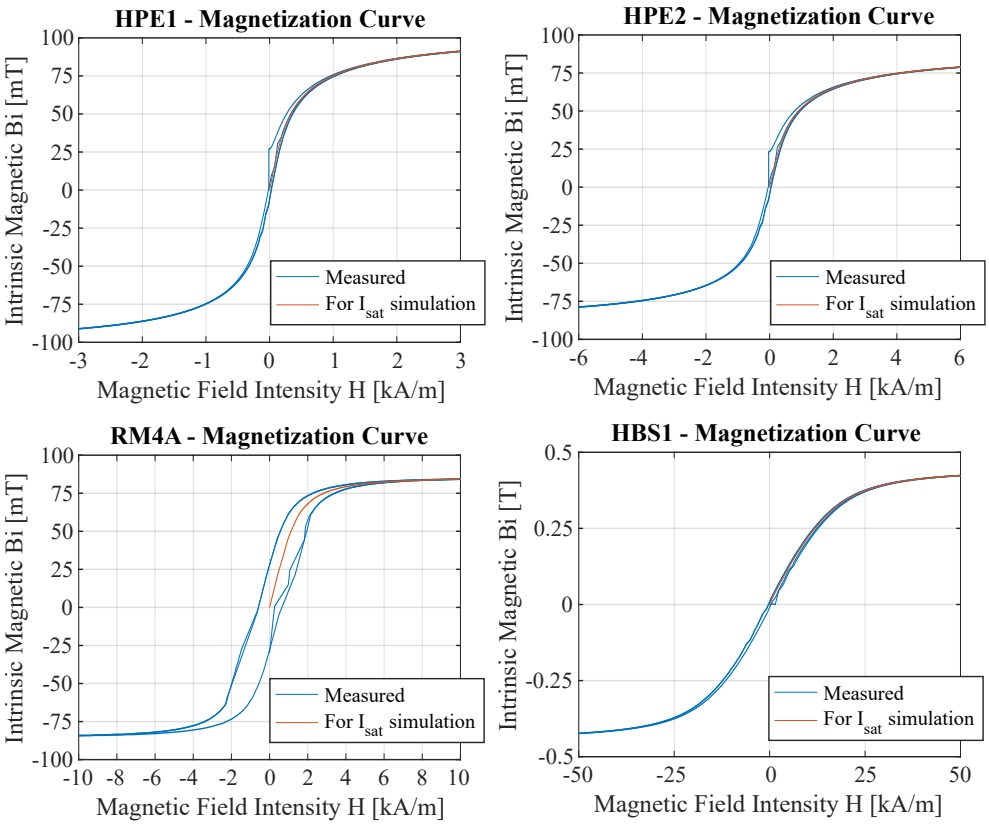


Figure 4.3: Material Bi-H curve.

4.3 Fabrication Process

Inductors with a high inductance density but low DC resistance entails a trade-off between the thickness and number of copper windings. Inductors with high inductance density can be easily achieved with a large number of windings. This inevitably leads to a large form factor and high DC resistance. Low resistance is imperative for power modules to reduce Joule heating and stresses induced in the package due to thermal loading.

By incorporating advanced magnetic composites as the core, the inductors can achieve high-inductance density without the need for a large number of windings. Magnetic-core inductors were designed for high conversion ratio converters and to ensure package embedding and thereby reduce interconnection lengths and associated parasitics. The inductor designs presented in this thesis were fabricated using a magnetic sheet as substrate and the process described in Figure 4.4.

First, a magnetic sheet is used as the substrate and ellipsoidal slots are drilled with an IR femto-second laser (steps 1 and 2). The IR femto-second laser thermally ablates the material removing it. The material evaporates in the form of plasma, creating the desired pattern. The slot drilling is controlled by optimizing the laser power, speed, and drill repetitions, and these parameters change from one material to another. For 100 μm and 200 μm material thickness, a single side drilling is enough when the parameters shown in Table 4.1 are used.

Table 4.1: Single side drilling parameters.

Parameter	HPE1	HPE2	RM4A	HBS1	MUE1	MUF1
Drilling step [μm]	-12	-12	-12	-12	-12	-12
Z step [μm]	-10	-10	-10	-10	-10	-10
Speed	80	80	80	80	80	80
Jump speed	200	200	200	200	200	200
Laser power	45	35	35	55	25	35
Repetitions	5	3	3	6	1	2

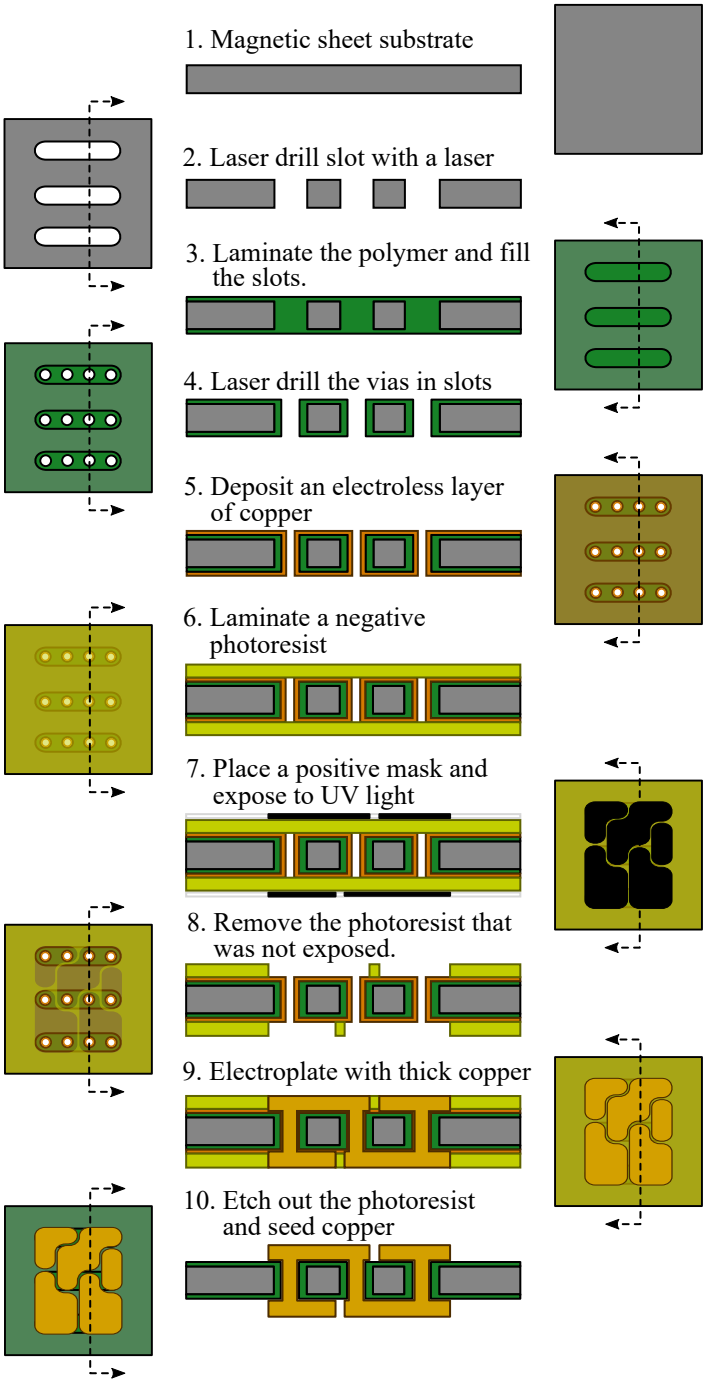


Figure 4.4: Fabrication process flow chart.

In step 3, the slots are filled with a 15 μm ABF^{TM} film for 100μm magnetic sheet thickness, and 30 μm ABF^{TM} film for 200μm magnetic sheet thickness, by hot pressing under vacuum at the viscoelastic temperature of the dielectric, allowing it to flow into the

slots. Thicker cores require thicker films to fill the slots completely in order to avoid voids and sagging of the dielectric within the slots. Next (step 4), the vias are laser drilled in the polymer-filled slots (vias-in-slot drilling). This allows to electrically isolate the vias and maximize their magnetic coupling. This via drilling process was optimized in a similar way as the slots.

In step 5, a thin layer of electroless copper seed layer is deposited. This is followed by ultraviolet lithography process, where a negative photoresist is laminated over the copper seed layer (step 6) and a positive mask is used to pattern the top and bottom layers (step 7). The photoresist is laminated using a hot roller. Vacuum lamination with hot press does not work because the photoresist flows inside the vias and gets stuck there and is not removed during the development. However, when using a hot roller air is trapped inside the via preventing it from clogging. Figure 4.5 shows the comparison of the results using vacuum lamination and the air bubble trapped inside the via using hot roller lamination.

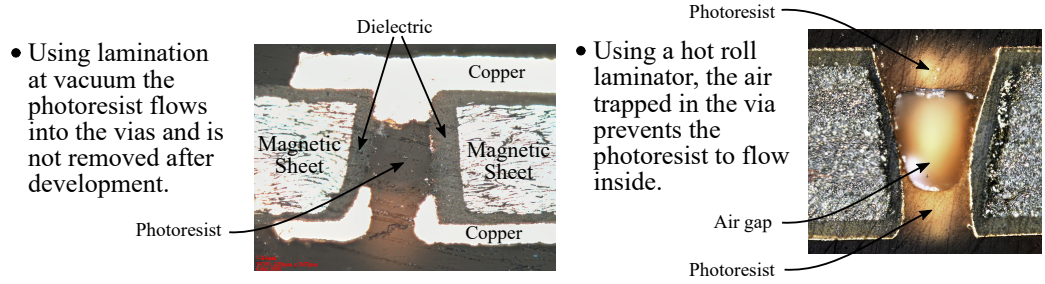


Figure 4.5: Comparison of photoresist lamination methods.

The photoresist that was not exposed is removed (step 8) and the inductor pattern become visible. Then the copper top layer, bottom layer, and vias are electroplated (step 9). The remaining photoresist is stripped, the plated copper is annealed to remove residual copper stress, and finally, the copper seed layer is etched using a differential etching process leaving behind the fabricated inductor (step 10).

4.3.1 Slot Drilling Optimization

For 400 μm thickness, slot drilling, slot filling, and via drilling need an extra step of optimization. It is not enough with a single side drilling due to excessive tapering, as shown in Figure 4.6. A 3-step double side drilling process was developed for 400 μm magnetic sheet thickness, as shown in Figure 4.7.

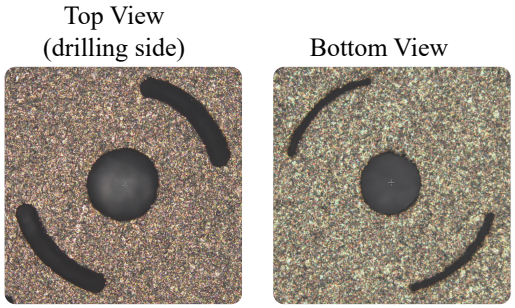


Figure 4.6: Single side drilling shows excessive tapering.

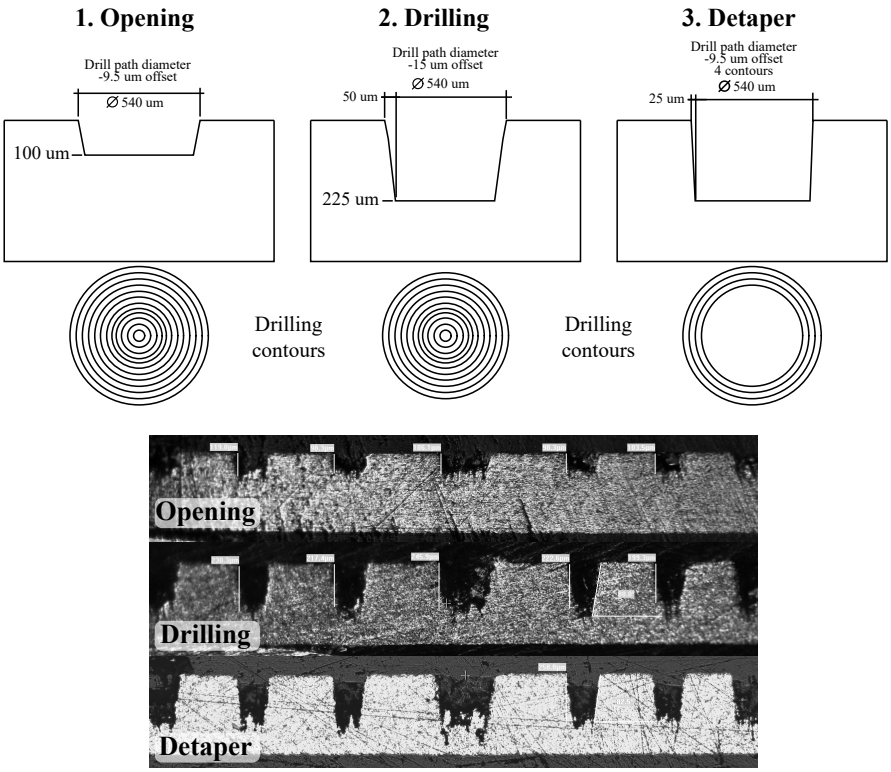


Figure 4.7: 3-Step double side drilling process.

First, an opening operation with low power and depth of 100 μm is used to define the

feature shape and size. Then, a drilling operation with more power but smaller features is used to drilling to a depth of 250 μm. Finally, a detapering operation where only 4 contours are drilled to reduce the taper and produce sharper edges.

4.3.2 Slot Filling Optimization

As the thickness of the substrate increases, it becomes difficult to completely fill the slots and at the same time avoid laminating a thick dielectric on both sides. Optimize the process to fill the slots is required to ensure i) slots are completely filled, ii) the right amount of material is used to not increase disproportional the substrate thickness, and iii) make sure the surface is planar.

The tests are conducted in a dummy FR4 substrate of 400 μm. In the first test 15 μm of ABF is hot press at vacuum with the conditions and results shown in Figure 4.8. As the figures show, with 15 μm it is not enough to fill all the slots, but also, all the material flows into them.

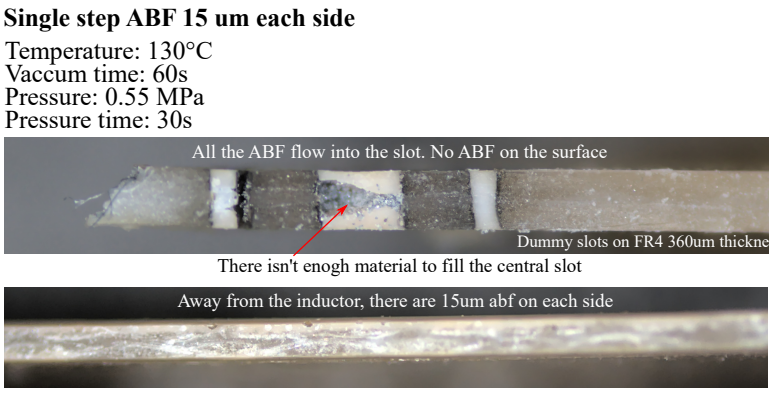


Figure 4.8: Slot filling test 1.

Next, in the second test, we tried with 30 μm ABF with the conditions and results shown in Figure 4.9. As the figure shows, with 30 μm most of the slots are completely filled, but there are still some gaps.

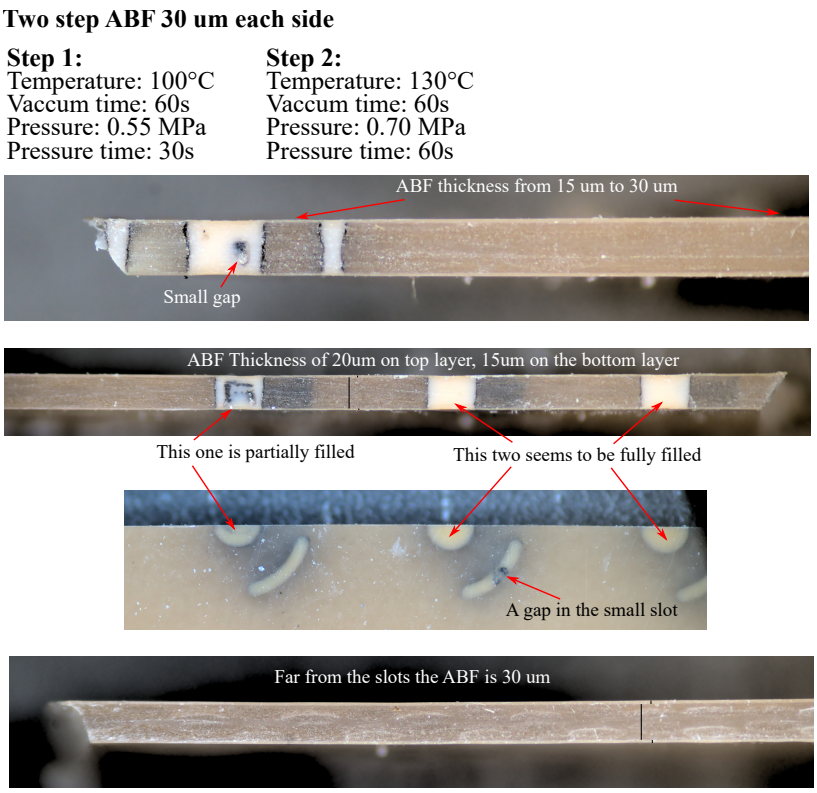


Figure 4.9: Slot filling test 2.

There is still some material on the surface that can make it flow into the gaps. Increasing the pressure time helped to completely fill the slots as shown in Figure 4.10.

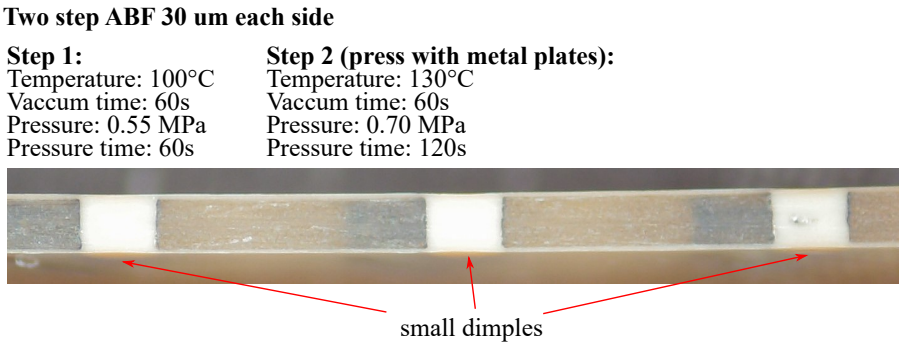


Figure 4.10: Slot filling test 3.

To ensure the planarity of the surface, first the ABF is cured, and then a 5 μm ABF is laminated again to obtain the result shown in Figure 4.11.

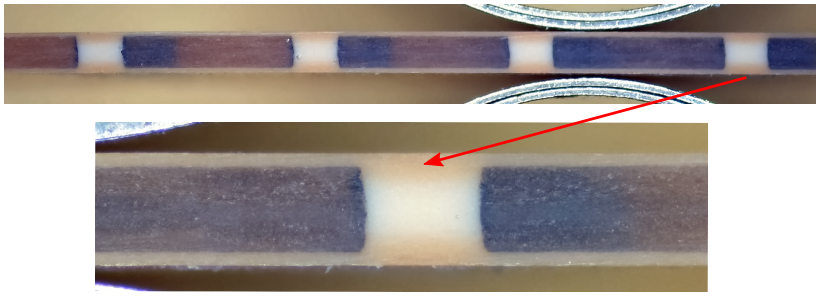


Figure 4.11: Slot filling test 4.

With the slot drilling and filling process optimized, the rest of the fabrication process can be carried out without any issues. Three batches of fabrications were completed, where each of them advances in complexity. In the first batch, three inductors (IND034, IND035, and IND036) were fabricated using HPE1 in a 100 μm magnetic sheet. In the second batch, 6 inductors (IND034, IND035, IND036, IND037, IND046, and IND047) were fabricated using the 6 materials (HPE1,HPE2, RM4A, HBS1, MUE1, and MUF1) in 400 μm magnetic sheets. Finally, in the third batch, an array of 16 inductors (IND048) were fabricated using HPE1, HPE2, and RM4A in 400 μm magnetic sheets. In the next sections, the fabrication and measurement results are presented.

4.4 First Batch

For the first fabrication batch, only inductor models IND034, IND035, and IND036 were considered. These inductors were simulated and designed at the earlier stage of this research and only the small signal measurement was performed. Figure 4.12 shows the inductor dimensions.

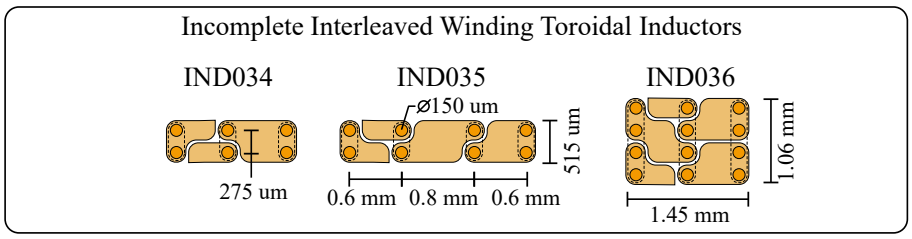


Figure 4.12: First batch.

The result of the fabrication of the first inductors is shown in Figure 4.13. These structures have the shunt measurement test points (compatible with 500 μm pitch GSG RF probes) as part of their design, and therefore, only the small signal shunt-thru measurement can be performed. It was designed in this way, avoiding the use of connectors or other measurement fixtures, to reduce the source of errors and validate the inductor technology and fabrication process.

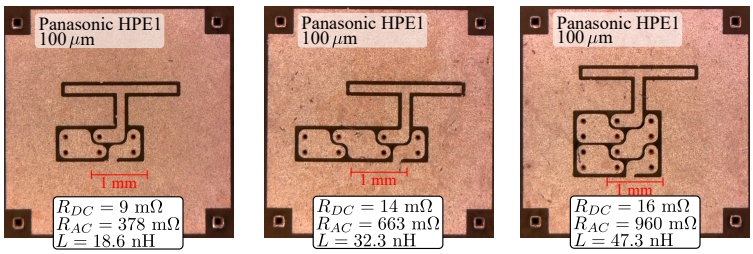


Figure 4.13: Top view of the first batch of inductors.

The cross section of the sample IND036 is shown in Figure 4.14 showing the magnetic material, the dielectric, and the through vias. The simulation model in ANSYS™ HFSS was adjusted to match the fabricated dimensions. The average copper thickness was 25μm.

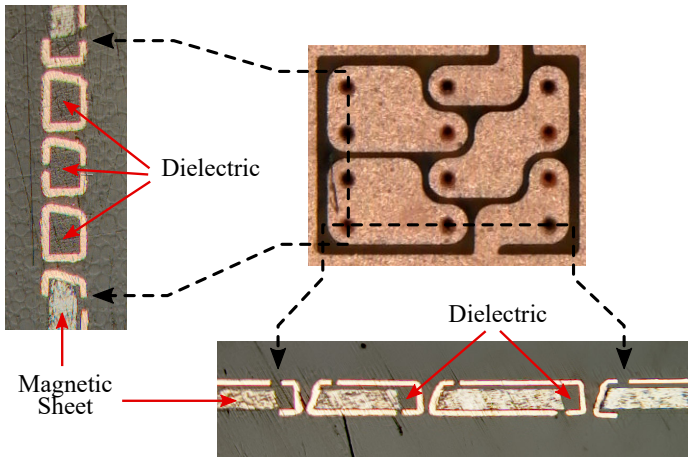


Figure 4.14: Cross section of IND036 from the first batch.

The small signal inductance and resistance spectra is shown in Figure 4.15. The correlation between measurement and simulation is very good. With a validated inductor

technology and fabrication process, we could then start to design a larger set of inductors along with a measurement fixture suitable for all the measurement methods presented in Chapter 3.

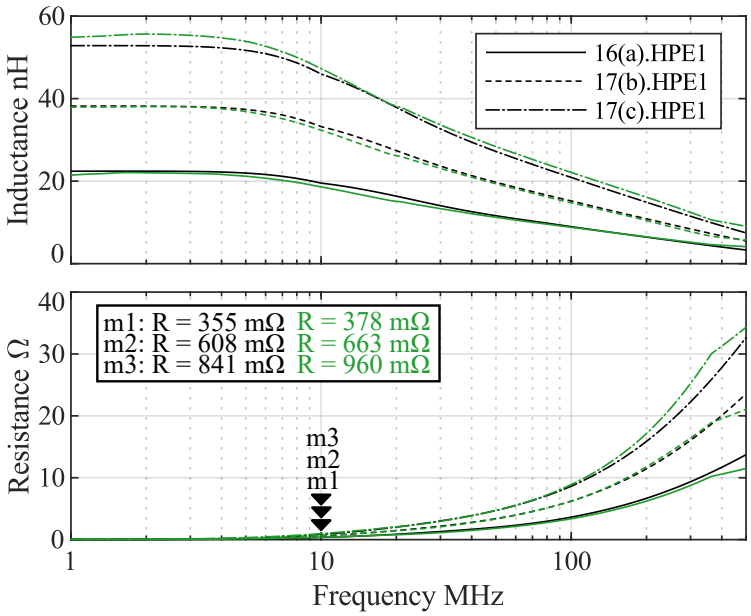


Figure 4.15: Small signal inductance and resistance spectra.

From these measurements, we can extract the small signal effective AC resistance per unit inductance. The small signal r_{acx} is computed with (Equation 3.16) and repeated here.

$$r_{acx} = \frac{2}{D^2(1-D)^2} \sum_{n=1}^{N} \frac{\sin^2(n\pi D)}{(n\pi)^4} \frac{R_{AC}(nf_s)}{L(f_s)}$$

The r_{acx} as a function of the duty cycle at different frequencies is shown in Figure 4.16. It is observed that the r_{acx} values are very close to each other for the different structures. This gave the first impression that this metric is invariant with inductance and geometrical changes. With the second and third batch of inductors, a larger number of different structures and materials were tested for both, technology comparison and the invariance of r_{acx} (and also the large signal R_{acx}).

It is also observed how the r_{acx} increases faster with duty cycles less than 20%. This shows the importance of the duty cycle extension provided by the hybrid power stage

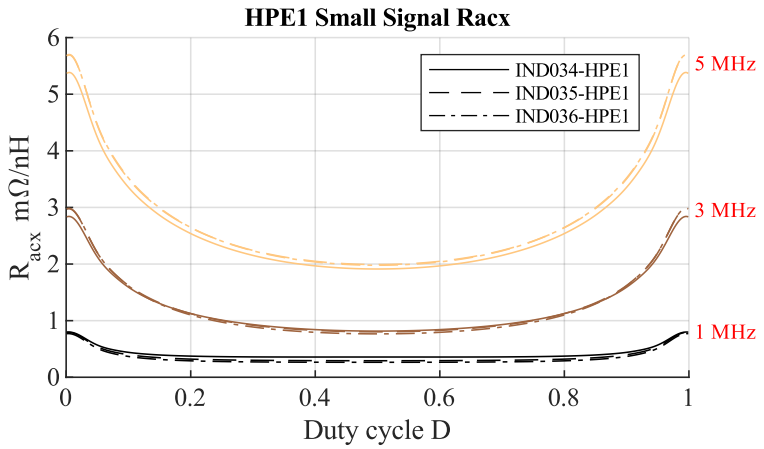


Figure 4.16: R_{acx} of first batch of inductors.

topologies. Topologies that cannot provide a high enough duty cycle, will produce too much losses in the inductor, greatly affecting the system efficiency.

4.5 Second and Third Batch

The first batch of inductors had the purpose of validating the inductor design and fabrication process, and was designed before we had the acknowledge of the r_{acx} properties and that we can use them to properly size the inductor. For the second and third batch, we consider a magnetic substrate with 400 μm to increase 4 times the inductance, along with some optimizations to further increase the inductance density while keeping a low DC resistance.

Even with material HPE1, the first inductor cannot give enough inductance. The inductance density can be increase if the central vias are arranged in a polar array. This reduces the magnetic path length, and therefore, increasing the inductance. At the center of Figure 4.17 it is shown the modification to IND036, this produces the design IND047. Since in a package IVR, the inductor output needs to be routed from the IVR package to the SoC package, and extra via must be placed somewhere to make this connection. This via can be placed, instead, right in the center of the inductor to further boost its inductance. The normal winding incomplete toroidal inductor with coaxial return via IND048 is shown in Figure 4.17

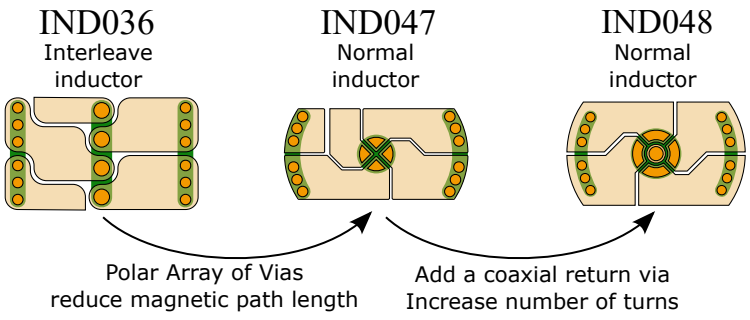


Figure 4.17: Inductor Optimization.

Figure 4.18 shows all the designs and dimensions included in the second fabrication batch. Fabricating all of them is required for a proper comparison of inductance, DC resistance, and losses.

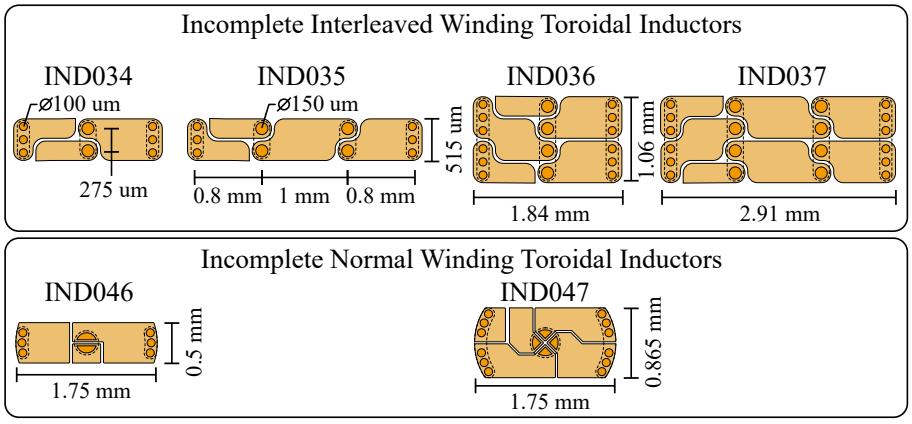


Figure 4.18: Second batch.

The first batch only allowed to measure the small signal inductance spectra. A different design was needed to extend measurements to include the large signal response. The fabrication results for the 2nd batch are shown in Figure 4.19. Each inductor has two 1 mm circular pads that are used to connect the inductor to the measurement fixture. Since these connections will add errors to the measurement, a Sort, Open, and Load (SOL) calibration structures were added in the backside of the sample. These calibration structures will be used to find the error box and de-embedd the inductor measurement. In the samples, it was also included in the center four vias drilled directly on the magnetic sheet (thus, in touch with the metallic fillers). In Table 4.2 it is shown the measured resistance between 1 mm

apart vias.

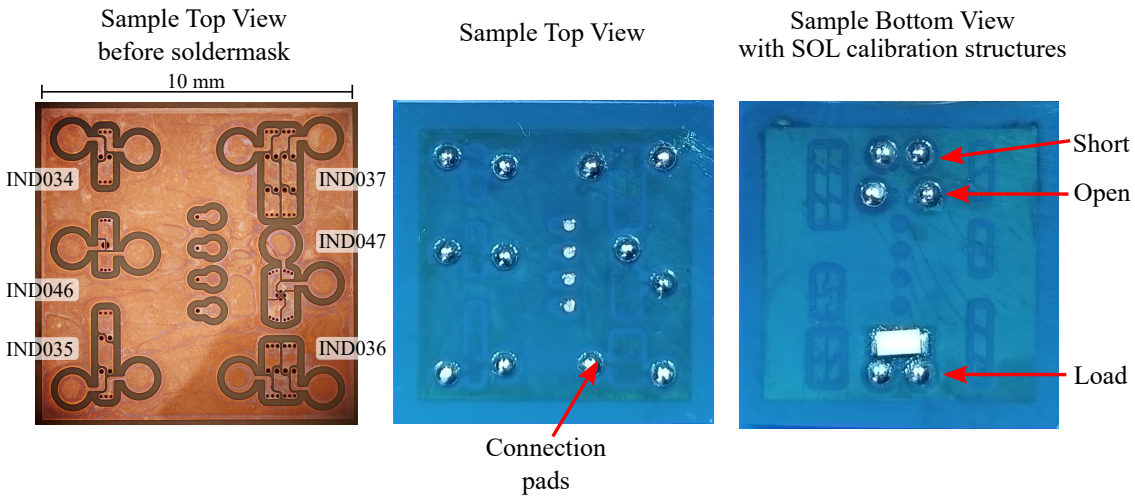


Figure 4.19: Second Batch of inductors.

Table 4.2: Magnetic material resistance between 1 mm apart vias.

HPE1	HPE2	RM4A	HBS1	MUF1	MUE1
5.5 Ω	27 kΩ	50 MΩ	Hi-Z	Hi-Z	Hi-Z

For the third batch, an array of 16 IND048 inductors in a 1 cm square was designed. The objective is to demonstrate that this technology can be used to developt multiphase IVRs with all the required inductors embedded on the same magnetic substrate.

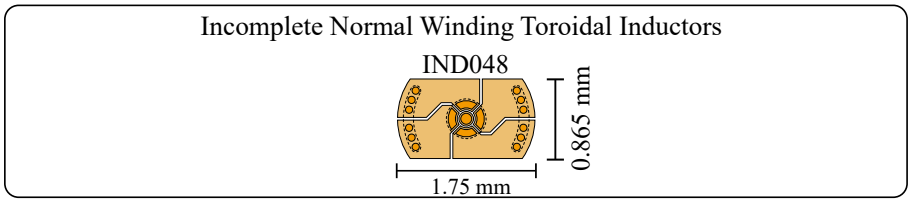


Figure 4.20: Third batch.

Figure 4.21 shows the different steps of the fabrication process. A second metal layer was required to connect the coaxial return via and expose the contact pads. Figure 4.22 shows the cross section around the central vias showing the result of the 3-step double-side drilling and the slot filling optimization: very low tapering, very well aligned vias, and fully filled slots.

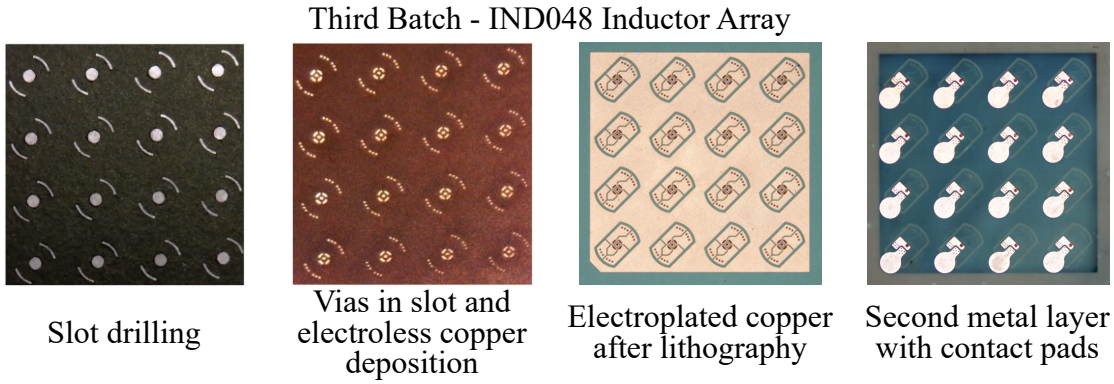


Figure 4.21: Third Batch of inductors IND048.

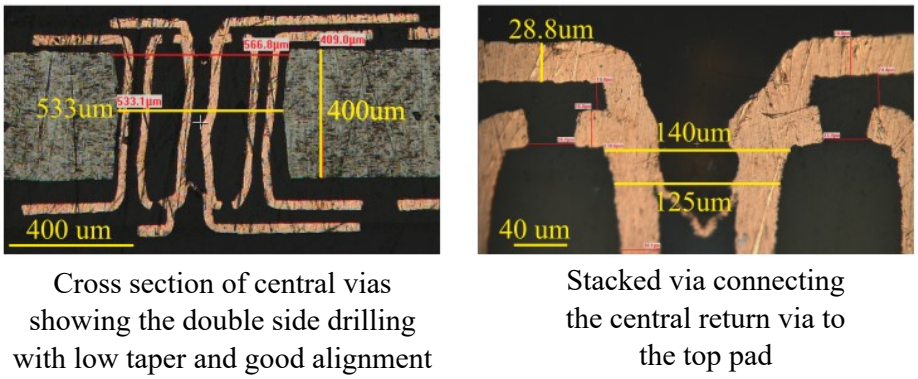


Figure 4.22: Cross section of IND048.

The next subsections show the measurement results for the small signal spectra without DC bias current in an extended frequency range from 100 kHz to 1 GHz, the small signal spectra with DC bias in the frequency range of 100 kHz to 100 MHz, and the large signal response. Reliability measurements such as aging with respect to thermal cycles and time-of-use in a buck converter with high currents were not performed and should be covered in a future work.

4.5.1 DC Resistance

The next Table shows the measured DC resistance, where the average copper thickness was 25 μm. The simulated DC resistance was fitted to the measurements to estimate a copper conductance of 4.2 S/m. With this conductance, to obtain a DC resistance close to 14 mΩ with inductor IND048 the copper thickness must be increased to 50 μm.

Table 4.3: Inductors DC resistance in mΩ with 25 μm electroplated copper thickness.

IND034	IND046	IND035	IND036	IND047	IND048	IND037
14.3	13.6	21.3	24.9	29.0	22.8	39.3

4.5.2 Small Signal Spectra

In Figure 4.23 and Figure 4.24, the small signal inductance and resistance spectra without DC bias current is shown. With the extended frequency range from 100 kHz to 1 GHz it is possible to obtain the close-to-DC, AC, and RF response. At 100 kHz we observe how the AC resistance converges to the DC resistance, a measurement that is only possible with a shunt-thru method. The 2-level calibration works very well and we see that the simulations (in the dash red lines) match very well the measurements (in solid blue lines), with the only exception of IND048 with HPE1 material where it measured 40 nH higher. We start to see a discrepancy at frequencies greater than 500 MHz for high inductance inductors, such as IND037, IND047, and IND048 with the low frequency material and for inductor IND037 with material HBS1. This can be attributed to higher parasitic capacitances, however, it is not very relevant to the inductor behavior above 500 MHz. We observe that with higher permeability, the lower is the operating frequency range.

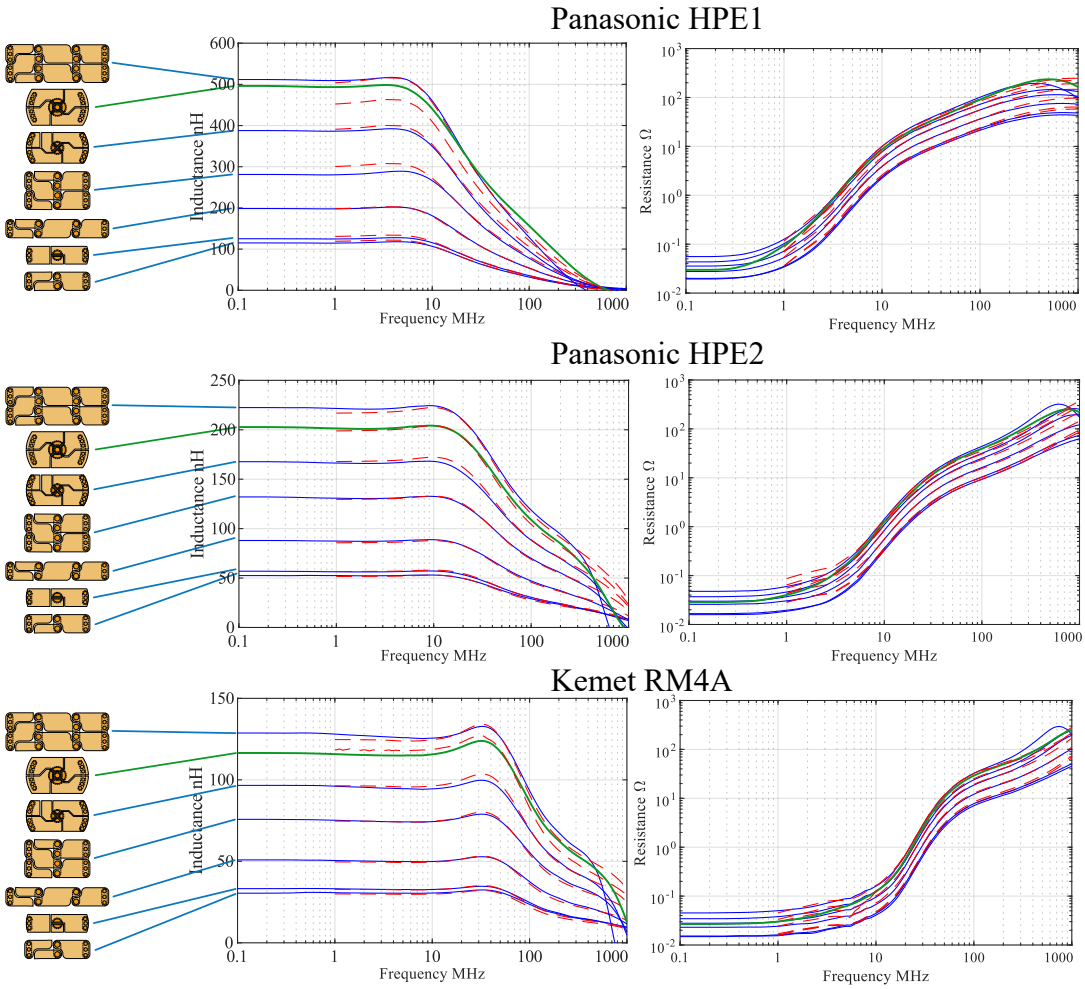


Figure 4.23: Second and third Batch of inductors. Low frequency materials.

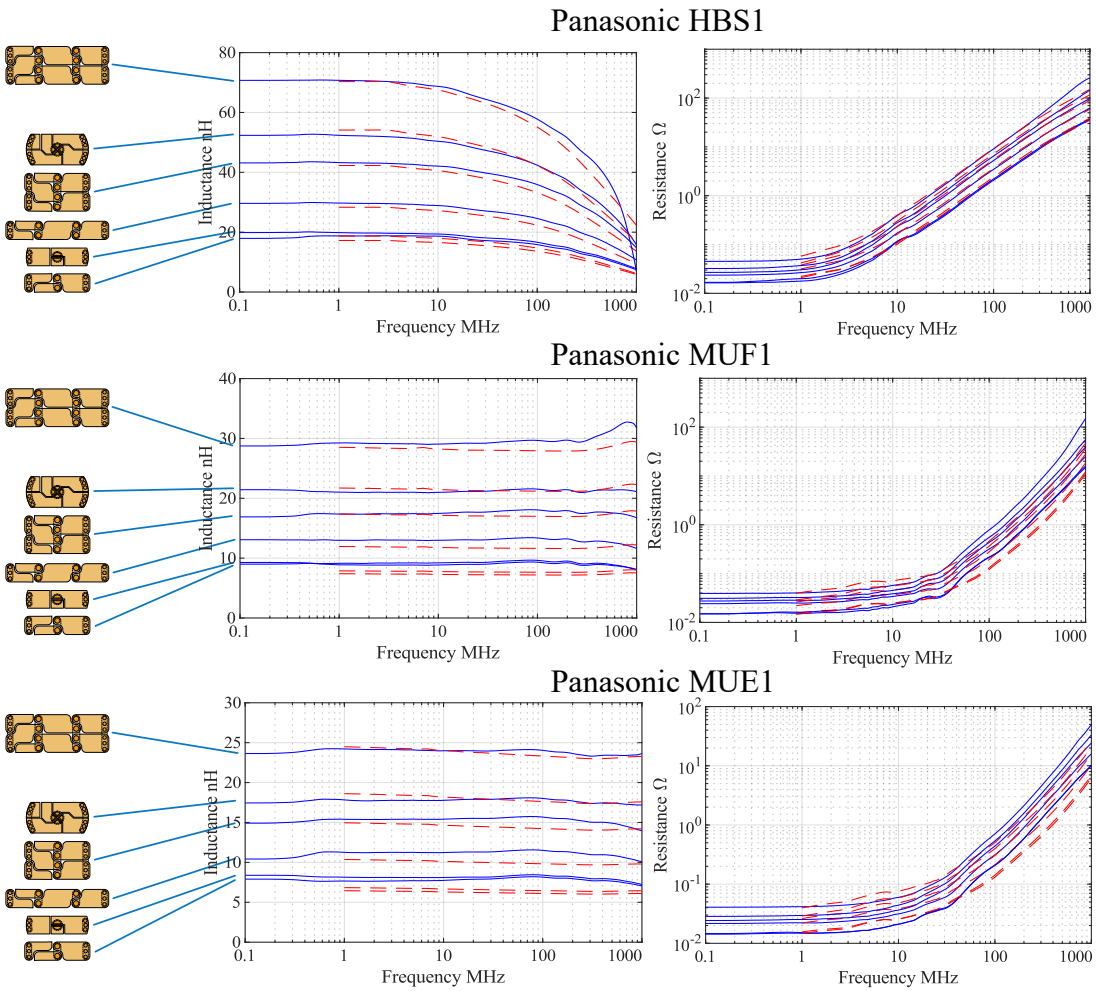


Figure 4.24: Second and third Batch of inductors. High frequency materials.

Using the measured small signal spectra of this large set of inductors, we can have a more extensive comparison of the small signal r_{acx}, as shown in Figure 4.25 (at each frequency, different lines correspond to a different inductor). We observed the invariant property in all the structures. Some discrepancies start to be visible for duty cycles less than 5%. With this metric, we can compare the small signal losses of each material. The materials HPE1, HPE2, and RM4A have flake fillers. The r_{acx} of HPE1 is the larger as it is the one with the highest permeability, but also a higher bulk conductivity. The material HPE2 has a lower bulk conductivity showing lower losses. In the case of RM4A, it has not bulk conductivity and therefore the small signal losses, due to eddy currents, are extremely low. The materials HBS1, MUE1, and MUF1 have spherical fillers. HBS1 is considered

a mid-frequency material, because above 20 MHz its r_{acx} starts to be large. The materials MUF1 and MUE1 can easily be operated at 50 MHz or above.

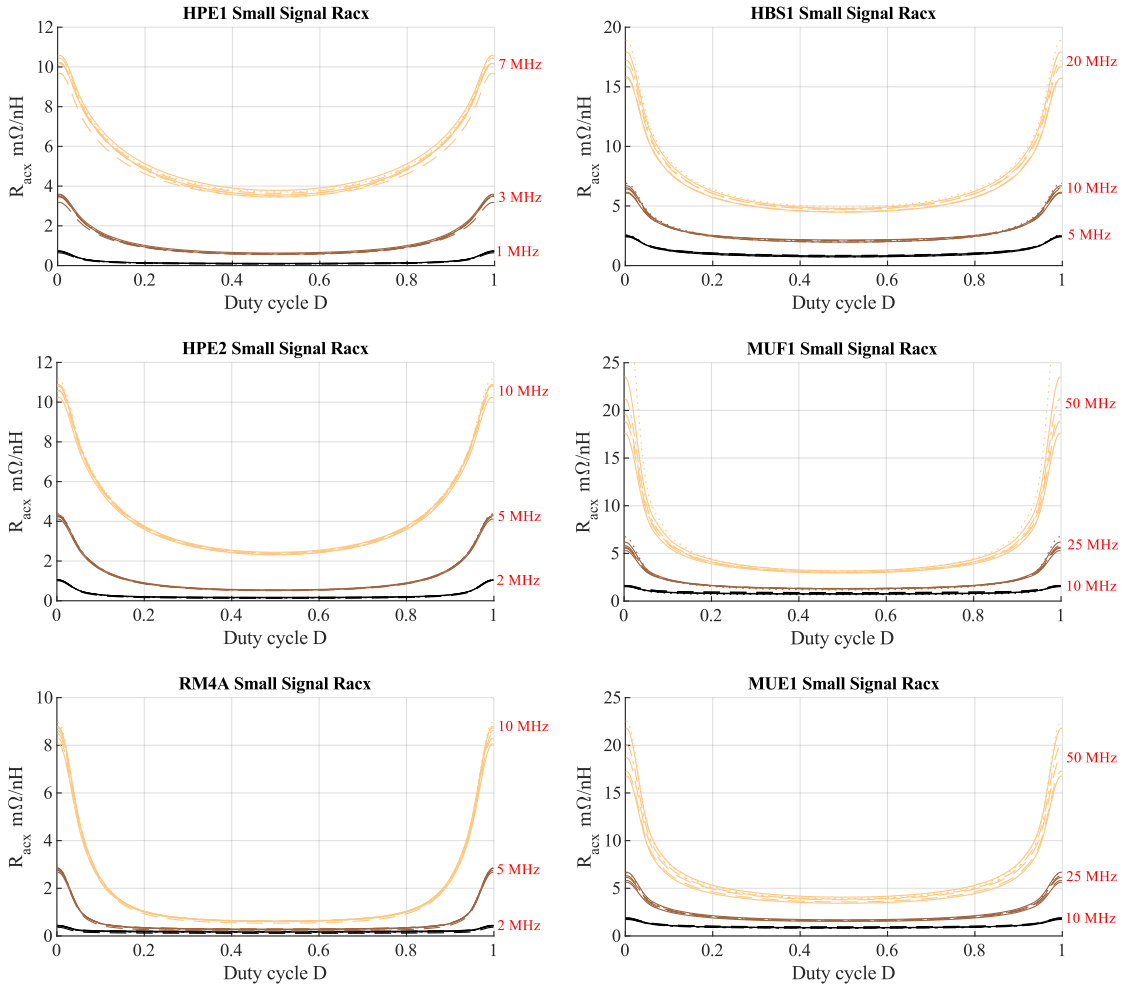


Figure 4.25: Small signal R_{acx}.

4.5.3 Small Signal Spectra with DC Bias Current

Using the test setup presented in Section subsection 3.7.2 it is possible to measure the small signal spectra with an applied DC bias current with very good precision. In Figure 4.26 and Figure 4.27 it is shown some of the measurements with the low frequency and high frequency materials, respectively.

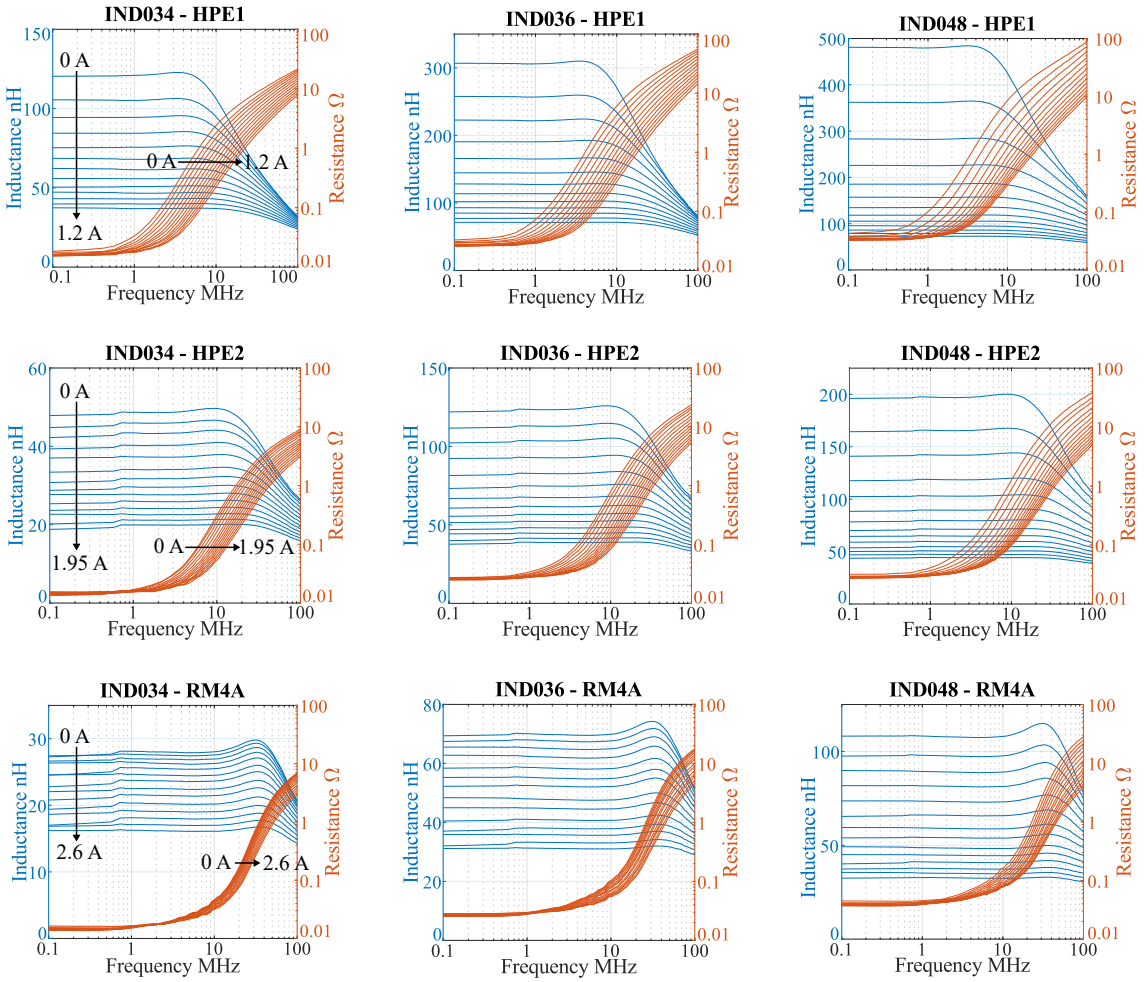


Figure 4.26: Small signal spectra with DC bias. Low frequency materials.

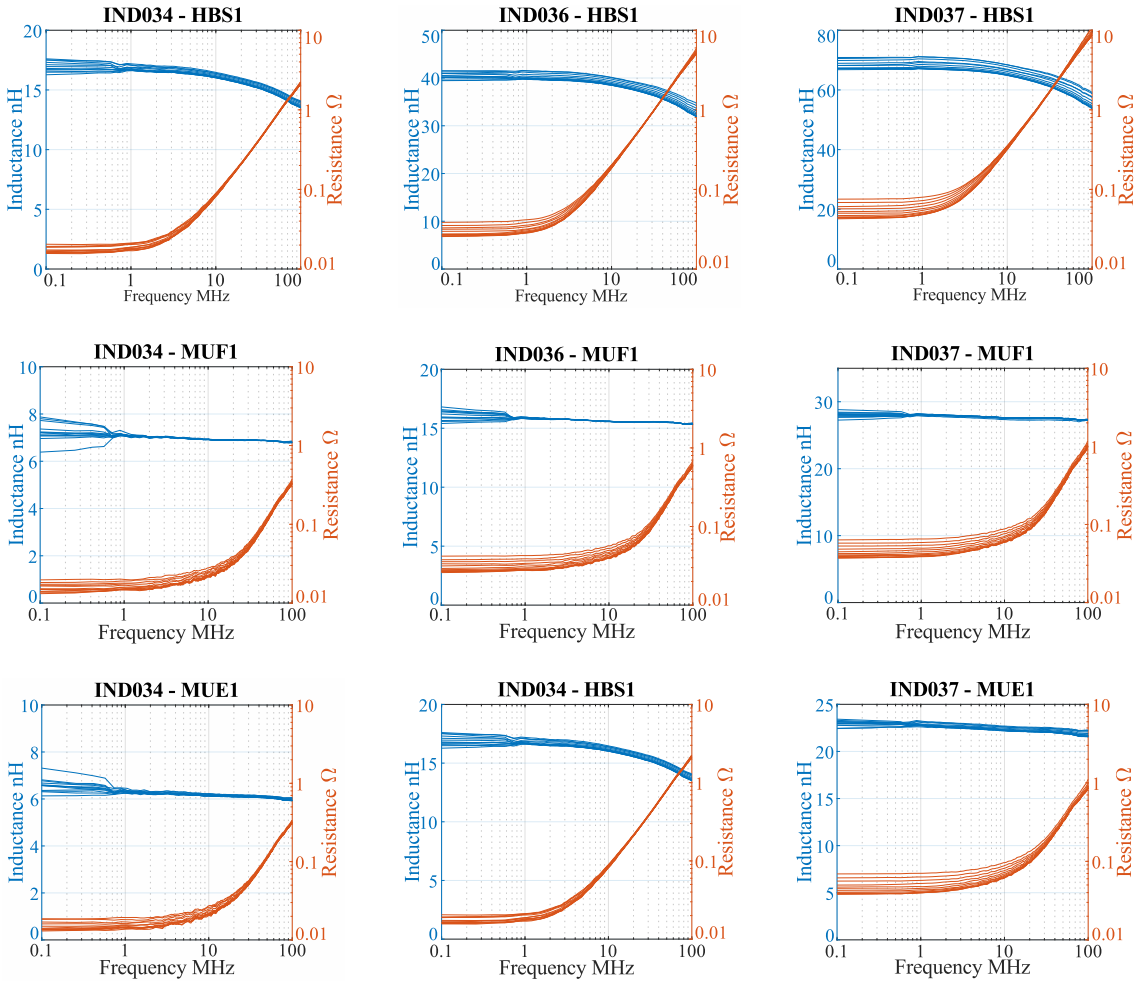


Figure 4.27: Small signal spectra with DC bias. High frequency materials.

We observe that the low frequency materials start to saturate as soon as a small current of 100 mA is applied. The dependency of the inductance as a function of the bias current is shown in Figure 4.28, where both the measurement and simulation results are shown.

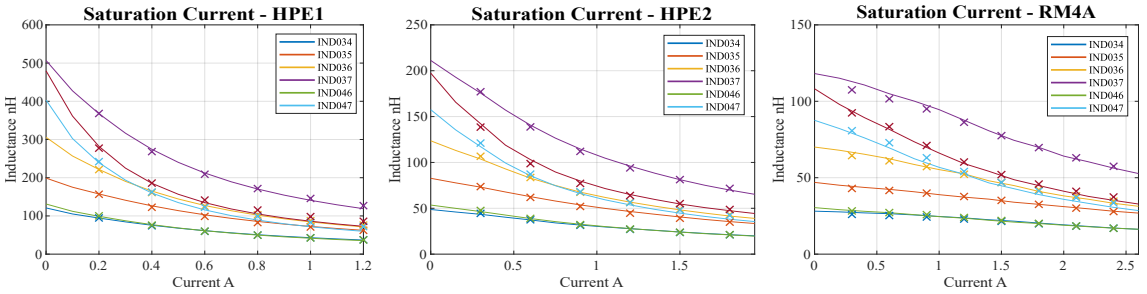


Figure 4.28: Small signal inductance as a function of the DC bias. Lines correspond to measurements and cross marks to simulation points.

Figure 4.29 shows their inductance and r_{acx} variation as a function of the DC bias current. Since r_{acx} is a measure of the eddy current losses, in materials HPE1 and HPE2 the small signal losses starts to decrease as the material becomes saturated as a consequence of a lower $d\phi(t)/dt$. However, in case of RM4A were the eddy current losses are already very small, the small signal losses are slightly higher at higher currents. This increment can be due to an increment of the temperature and resistance due to Joule heating. With the small-signal measurements, the magnetic hysteresis losses at not included, and the temperature only have an effect on the copper resistance and magnetic conductivity. The resistance dependency of a positive temperature coefficient (PTC) conductor is given by,

$$R_T = R_{ref}[1 + \alpha(T - R_{ref})] \tag{4.5}$$

where α if the temperature coefficient with units of percentage per unit of temperature (i.e. %/°C), T if the current temperature and T_{ref} is the temperature at which the R_{ref} was measured. With temperatures $T > T_{ref}$ the resistance will increase, therefore, increasing the losses in the copper and reducing the losses in the magnetic materials. If the increase of copper losses is higher than the reduction of magnetic losses we will have a net increment of losses increasing the r_{acx} value, and this is what happens with RM4A material. With respect to the hysteresis losses, in [67] and [68] it is shown that they are lower at higher temperature.

This very low saturation point prevents any of these materials to be used in a buck converter, because only the inductor current ripple can be up to 500 mA. It is well known that air-gaps can increase the saturation current, but for embedded inductors, it is required magnetic materials with engineered distributed air-gaps. The high frequency materials with spherical fillers have this property.

Figure 4.30 shows the inductance and r_{acx} variations as a function of the DC bias current for all the high frequency materials. For these three materials, the saturation current is

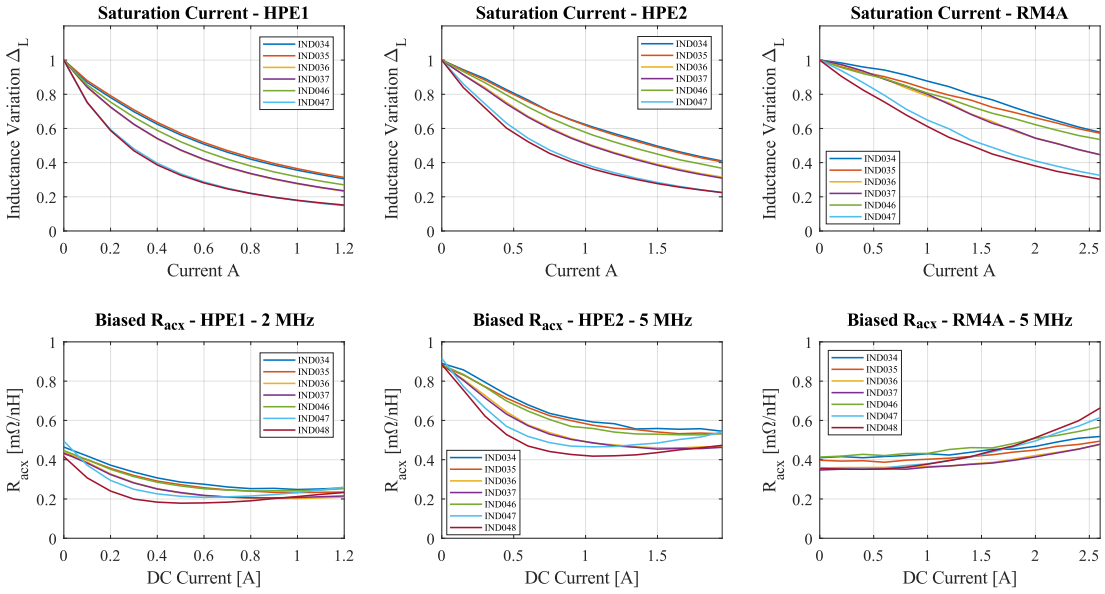


Figure 4.29: Small signal R_{acx} with DC bias. Low frequency materials.

above 5 A. The apparent increase of inductance is due to the error introduced by the 6.8 μH DC current source filter inductors that start to saturate at currents close to 5 A. We observe that at currents higher than 2 A, the DC resistance starts to increase due to Joule heating, this also produces an increment in the r_{acx}. These materials are fabricated using spherical fillers in a polymer matrix. As result, between each spherical particle there are small gaps that act as distributed "air-gaps" decreasing the effective permeability, linearizing the BH hysteresis loop, and increasing the saturation current.

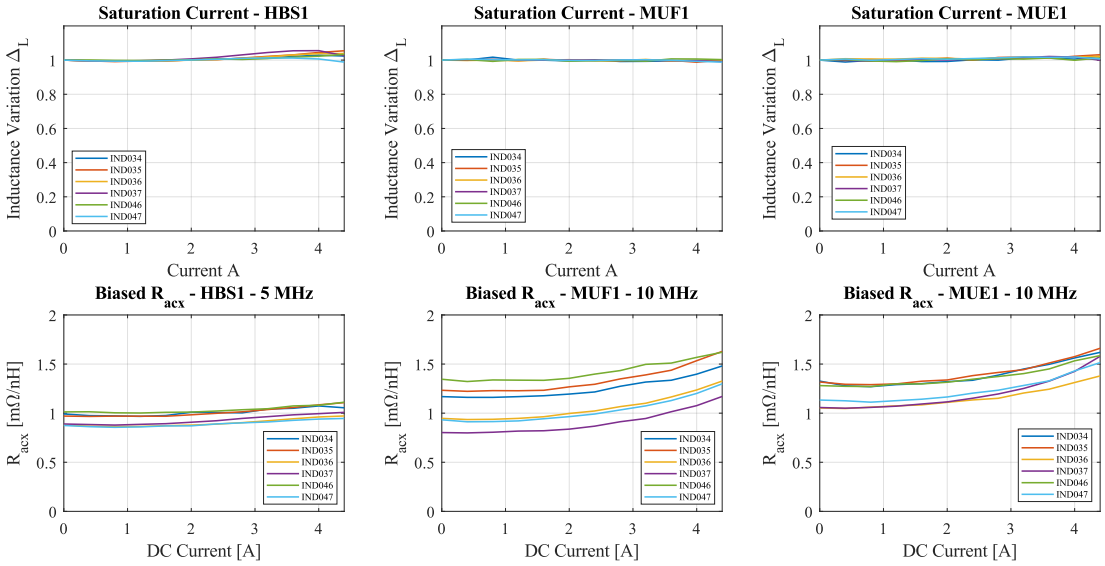


Figure 4.30: Small signal R_{acx} with DC bias. High frequency materials.

4.5.4 Large Signal

To study the large signal response, The inductors IND036 with HPE2 and IND037 with HBS1 were analyzed with the setup shown in Section subsection 3.7.3, where the inductor is placed in a buck converter with 0 DC load current allowing to easily measure the large AC signal response. By capturing the inductor voltage and current waveform, we can isolate the inductor losses from the losses of any other component. Three different measurement sweeps were performed: current ripple with constant duty cycle, duty cycle with constant current ripple, and frequency. These three measurements sweep allows us to determine up to what degree the R_{acx} remains constants or how it changes according to the parameter sweep.

Current Ripple Sweep

Figure 4.31 shows the recorded waveforms for the current ripple sweep for both inductors, and Table 4.4 and Table 4.5 show the extracted parameters. For HPE2 we observe that, with as little as 80 mA, the extracted inductance is already different from what is expected. The average inductance is apparently large, but this is because of a lower di/dt produced by a

larger L/R time constant (due to large hysteresis losses). With a saturated magnetic core, the relation between the small and large signal R_{acx} is not valid. In the case of HBS1, the inductance values are correct over the entire current ripple sweep (the connection wires add some inductance). The large to small R_{acx} ratio is almost constant with an average factor of 5.1, this shows that the small and large signal losses seem to be related by a constant, at least in a narrow frequency band and current ripple.

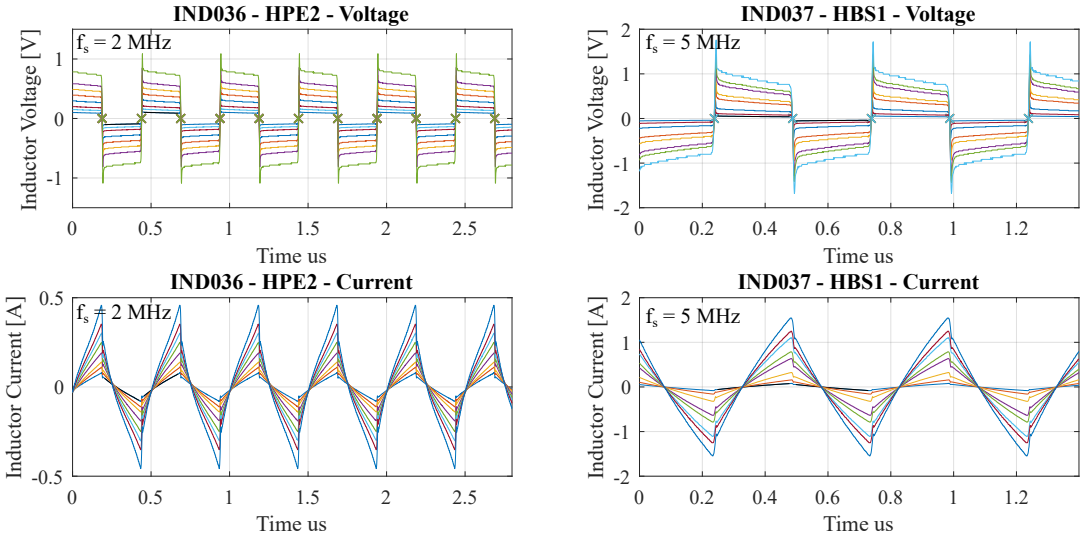


Figure 4.31: Large Signal Current Ripple Sweep.

Table 4.4: Inductor IND036 - HPE2 parameters from large signal current ripple Δi_L sweep at $f_s = 2$ MHz. L_{sm} corresponds to the small signal inductance.

L_{sm}	nH	130.4	130.4	130.4	130.4	130.4	130.4	130.4	130.4
r_{acx}	$\frac{\text{m}\Omega}{\text{nH}}$	0.146	0.146	0.146	0.146	0.146	0.146	0.146	0.146
L	nH	171.2	197.0	199.3	221.5	232.7	244.8	255.6	273.3
Δi_L	mA	81.30	111.8	140.2	191.1	250.0	302.8	351.6	457.3
P_{AC}	mW	1.312	3.024	5.513	12.59	23.66	37.30	53.85	96.86
R_{acx}	$\frac{\text{m}\Omega}{\text{nH}}$	1.160	1.294	1.406	1.558	1.626	1.661	1.704	1.694
Ratio	$\frac{R_{acx}}{r_{acx}}$	7.930	8.851	9.618	10.652	11.123	11.360	11.655	11.587

Table 4.5: Inductor IND037 - HBS1 parameters from large signal current ripple Δi_L sweep at $f_s = 5$ MHz. L_{sm} corresponds to the small signal inductance.

L_{sm}	nH	69.8	69.8	69.8	69.8	69.8	69.8	69.8	69.8
r_{acx}	$\frac{\text{m}\Omega}{\text{nH}}$	0.753	0.753	0.753	0.753	0.753	0.753	0.753	0.753
L	nH	77.06	76.98	75.62	75.84	75.65	76.28	76.48	76.22
Δi_L	mA	77.24	149.4	227.6	300.8	373.9	447.2	513.2	584.4
P_{AC}	mW	1.656	6.609	14.95	26.55	41.63	59.87	80.09	105.2
R_{acx}	$\frac{\text{m}\Omega}{\text{nH}}$	3.602	3.847	3.814	3.869	3.934	3.925	3.976	4.043
Ratio	$\frac{R_{acx}}{r_{acx}}$	4.786	5.112	5.068	5.141	5.227	5.215	5.283	5.372

Duty Cycle Sweep

Figure 4.32 shows the recorded duty cycle sweep waveforms for both inductors. For HPE2 the current ripple was limited to 40 mA, and for HBS1 to 256 mA. In Table 4.6 and Table 4.7 it is shown the extracted parameters, for both materials. For HPE2 we observe that ratio R_{acx}/r_{acx} is almost constant with respect to the duty cycle with an average value of 6.3, showing that as long as the magnetic core is not saturated, the small and large signal losses are related by a constant. Similarly, for material HBS1, the small to large signal losses are related by an average constant of 5.1.

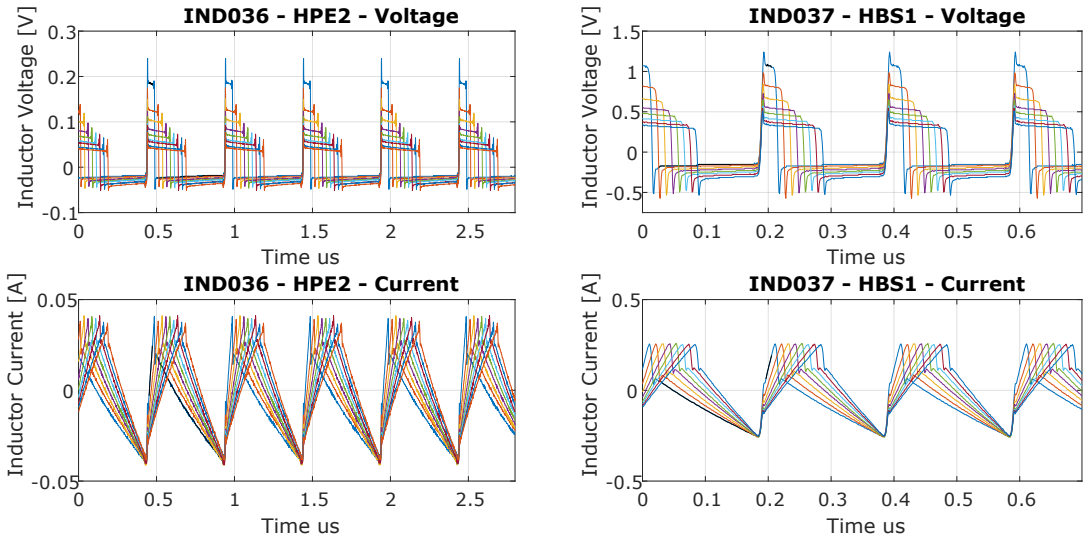


Figure 4.32: Large signal duty cycle sweep.

Table 4.6: Inductor IND036 - HPE2 parameters from large signal duty cycle D sweep at $f_s = 2$ MHz. L_{sm} corresponds to the small signal inductance.

D		0.15	0.20	0.25	0.30	0.35	0.40	0.45	0.50
L_{sm}	nH	130.4	130.4	130.4	130.4	130.4	130.4	130.4	130.4
r_{acx}	$\frac{\text{m}\Omega}{\text{nH}}$	0.217	0.186	0.169	0.159	0.153	0.149	0.147	0.146
L	nH	152.1	151.4	148.5	148.4	147.8	149.3	148.0	148.5
Δi_L	mA	39.13	41.16	40.65	40.65	39.63	41.16	37.60	38.11
P_{AC}	mW	0.285	0.304	0.273	0.258	0.233	0.245	0.199	0.199
R_{acx}	$\frac{\text{m}\Omega}{\text{nH}}$	1.222	1.184	1.113	1.051	1.002	0.969	0.951	0.922
Ratio	$\frac{R_{acx}}{r_{acx}}$	5.620	6.368	6.579	6.596	6.546	6.495	6.471	6.303

Table 4.7: Inductor IND037 - HBS1 parameters from large signal duty cycle D sweep at $f_s = 5$ MHz. L_{sm} corresponds to the small signal inductance.

D		0.15	0.20	0.25	0.30	0.35	0.40	0.45	0.50
L_{sm}	nH	69.9	69.9	69.9	69.9	69.9	69.9	69.9	69.9
r_{acx}	$\frac{\text{m}\Omega}{\text{nH}}$	1.086	0.969	0.892	0.838	0.799	0.773	0.758	0.753
L	nH	77.94	76.12	75.54	76.05	76.46	75.99	75.88	75.55
Δi_L	mA	256.1	256.1	256.1	256.1	258.1	252.0	254.1	252.0
P_{AC}	mW	28.15	25.77	23.87	21.85	20.79	19.39	18.65	18.40
R_{acx}	$\frac{\text{m}\Omega}{\text{nH}}$	5.507	5.161	4.819	4.381	4.081	4.016	3.808	3.835
Ratio	$\frac{R_{acx}}{r_{acx}}$	5.072	5.326	5.402	5.229	5.106	5.195	5.027	5.096

4.6 Large and Small Signal Losses Relation

After gathering all the large and small signal data, we can compare their relationship. The duty cycle sweep was recorded, for both materials, at frequencies 2, 3, 4, and 5 MHz (keeping the current ripple constant and below the saturation level). After extracting the large signal R_{acx}, the ratio $\kappa = R_{acx}/r_{acx}$ was computed as shown in Table 4.8. For frequencies above 4 MHz, in both materials the ratio κ seems to converge to a constant value.

Using the ratios shown in Table 4.8, Figure 4.33 and Figure 4.34 show the relationship between $\kappa\, r_{acx}$ (indicated by solid lines) and R_{acx} (indicated by the cross marks).

Table 4.8: Large to small loss ratio κ as a function of frequency at $D = 0.5$.

f_s [MHz]		2	3	4	5
HPE2	κ	5.900	7.344	7.464	7.011
HBS1	κ	3.074	4.134	4.806	5.069

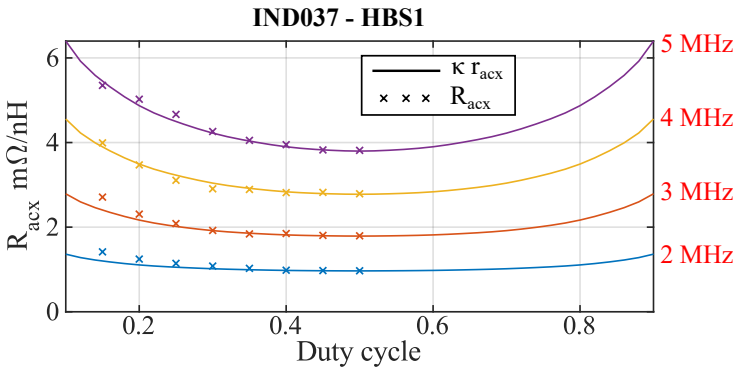


Figure 4.33: Large signal R_{acx} of HBS1 material.

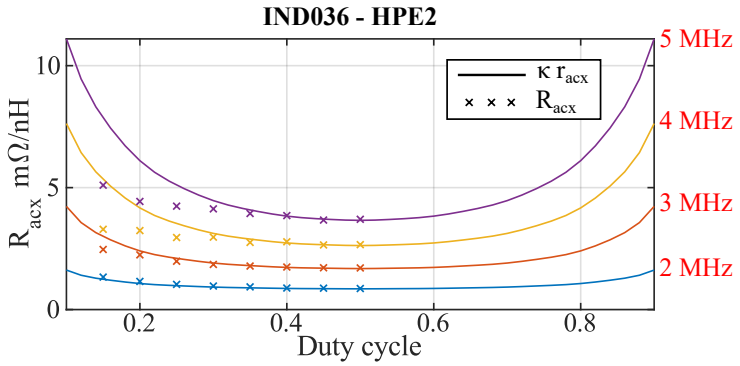


Figure 4.34: Large signal R_{acx} of HPE2 material.

With HBS1, we observe that the large signal losses follow the same behavior of the small-signal ones. However, for HPE2 and frequencies above 4 MHz, the large signal losses do not follow the same trend at low duty cycles. We think this can be due to the proximity of the switching frequency f_s to the f_{FMR} of the material, which is around 10 MHz for HPE2.

From these measurements, we can observe that the large signal is approximately proportional to the small-signal by a constant, at least in a narrow frequency band and duty

cycles between 0.15 to 0.85 (due to symmetry with respect to $D = 0.5$), then

$$R_{acx} = \kappa\, r_{acx} \tag{4.6}$$

In an extended frequency range, we can expect to get at DC the value of $\kappa = 1$ and at high frequencies $\kappa = K$. Let's consider the next modified sigmoid function as follow,

$$\kappa = \frac{K}{1 + (K-1)e^{\alpha f^{\beta}}} \tag{4.7}$$

where K is the maximum value of κ, and α and β are constants used to adjust the frequency position and slope, respectively. This function can give a reasonable expectation value for κ as shown in Figure 4.35. However, more experimentation is needed to know its actual behavior at lower and higher frequencies.

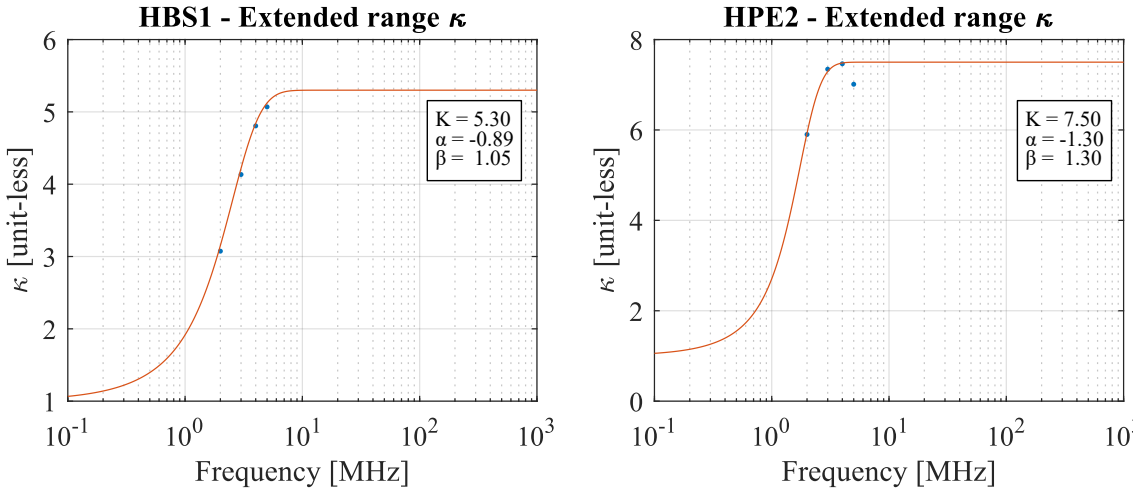


Figure 4.35: Extrapolation of the large to small signal κ.

If we compare the extrapolated factor κ with the inductor AC resistance, as shown in Figure 4.36, we can see that the change of its value coincides with the interval when it moves from a copper dominant losses to a magnetic dominant losses.

Based on this observation, it can be possible to estimate the inductor power loss at some

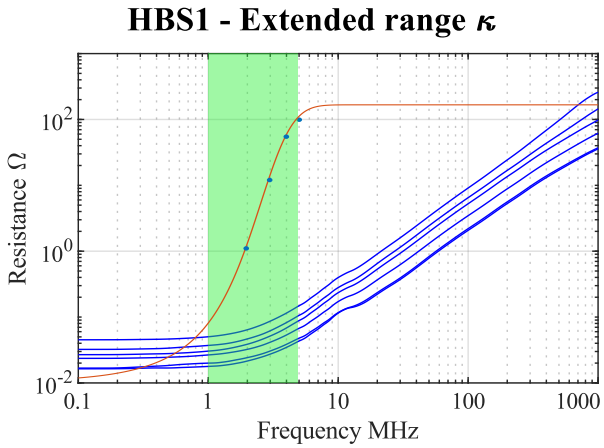


Figure 4.36: Relation between κ and the inductor AC resistance.

duty cycle D and switching frequency f_s with the next expression,

$$P_L = I_{DC}^2 R_{DC} + \Delta i_L^2 L\, \kappa(f_s)\, r_{acx}(D, f_s) \tag{4.8}$$

with r_{acx} given by (Equation 3.16). For example, with $\kappa = 5.1$ and an embedded inductor with inductance 100 nH (regardless of its size) using HBS1, we can predict the AC power loss surface of this material as shown in Figure 4.37. With $L = 100$ nH, $\Delta i_L = 0.5$ A, duty cycle of 0.2, and $f_s = 5$ MHz, the AC power loss would be 135 mW.

A more useful calculation gives the possible conversion ratios given a magnetic material. Using the AC power loss expression (Equation 3.30) and repeated here,

$$P_{L,AC} = \frac{V^2(1-D)^2}{4Lf_s^2} R_{acx}(D, f_s)$$

we can write the non-linear function $F(D)$ as follow,

$$F(D) = \frac{V^2(1-D)^2}{4Lf_s^2} R_{acx}(D, f_s) - P_{L,AC} = 0 \tag{4.9}$$

and solve for D for a given AC power loss $P_{L,AC}$. This will give us the allowed conversion

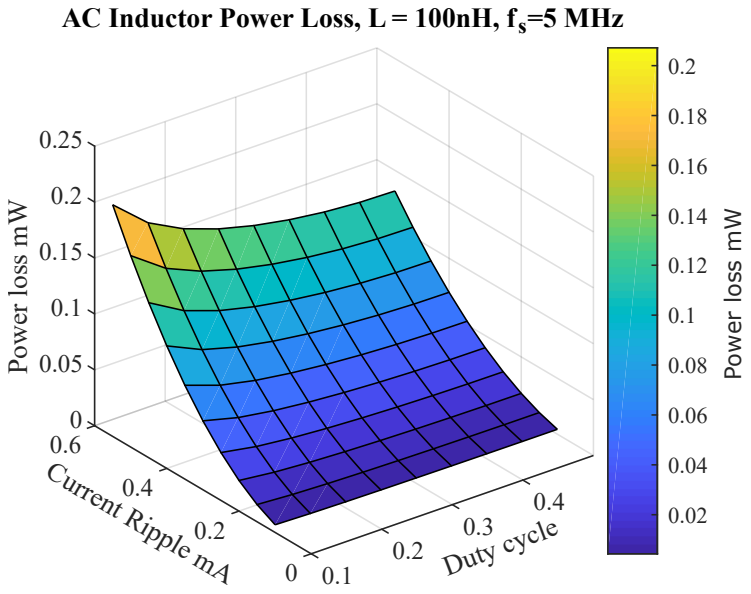


Figure 4.37: AC inductor power loss surface at 5 MHz.

ratios for a given inductor efficiency. The inductor efficiency is,

$$\eta_L = \frac{I_L V}{P_{L,AC} + I_L^2 R_{DC} + I_L V} \tag{4.10}$$

For example, Figure 4.38 shows the conversion ratio space for material HBS1 considering an inductance of 65 nH (as obtained with IND048).

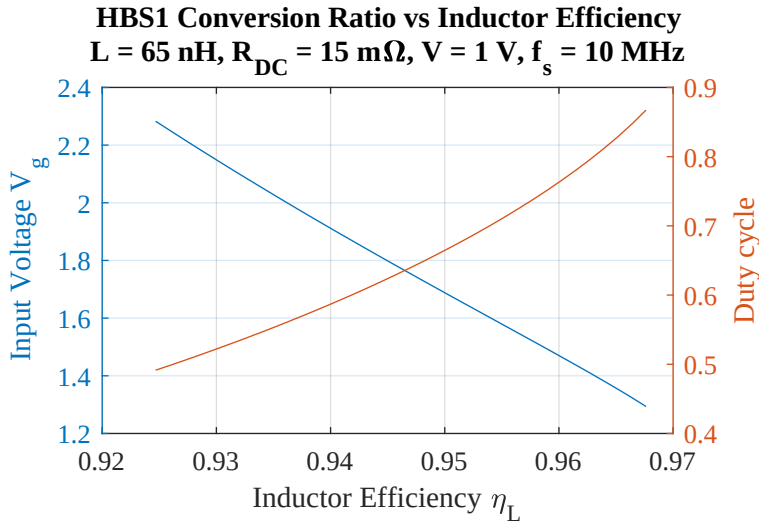


Figure 4.38: Conversion ratio space for HBS1 with $I_L = 1.875$ A. The efficiency includes the total inductor losses.

The high hysteresis losses and low inductance prevent the HBS1 material to be used for high conversion ratio applications. Its optimum conversion ratio at 10 MHz is 1.7 V to 1 V (provided the DC resistance is reduced to 15 mΩ), allowing an output current up to 5 A with an efficiency of 92%, and with maximum efficiency of 95% at $I_L = 1.875$ A.

In the following Chapters, it will be shown that we can extract a similar result for R_{acx} and r_{acx} using a simple discrete toroidal inductor. This discrete inductor only takes a day to be fabricated in contrast to the several months of work for the embedded inductors. This allows faster research of magnetic material targeted for embedded applications.

4.7 Comparison to State of the Art

This inductor design framework, where the inductor properties are determined to satisfy a target inductor efficiency, allows understanding the limitations of the magnetic materials and inductor technology. Table 4.9 shows the comparison of inductor model IND048 with material HBS1 to published embedded inductors with high inductance and low frequency. From the inductor technology point of view, we observed a higher L/R_{DC} ratio and a higher maximum current compared to other compact embedded inductors such as [24] and [25]. Thin-film inductors such as [69] can achieve very high inductance density but with very high DC resistance and very low current, limiting their application to low power devices. Non space-constrained inductors such as [18] and [19] can achieve a low DC resistance and high Q but at expense of inductance density, and therefore not suitable for IVRs.

We believe that by combining the latest inductor model IND048 with better magnetic material, the requirements for high voltage conversion ratio converter can be met. In Chapter 6, we use the inductor design framework to determine the required magnetic properties.

For a pure inductor technology comparison, in Table 4.10 the inductor IND048 with HPE1 is compared against other published inductors.

Table 4.9: Comparison of properties with state of the art embedded inductors for integrated voltage regulators. † Small signal quality factor Q.

Property		This work HBS1-IND048	Spiral [18] APEC 2018	Spiral [24] APEC 2019	Toroid [25] TPE 2019	Solenoid [69] APEC 2020	Toroid [19] CIPS 2020
Area	mm^2	6	225	13	5.76	0.9	110
Thickness	μm	600	1100	288	280	$<$100	500
Material μ_r		24	180	–	3	800	34
Material Type		MPC	MPC	Fe comp.	Ni-Zn comp.	Thin-Film	Fe comp.
Switching Freq.	MHz	10	2	16	12	10	2
Inductance L	nH	60.7	685	150	112	75	925
Inductance Density	nH/mm^2	12.1	3	11.5	19.4	83	8.4
DC Resistance	mΩ	22.8	40.7	205	265	270	66
Saturation current	A	5	–	1	1.6	0.40	5
I_{DC} @ 150 mW	A	2.56	1.92	0.855	0.752	0.745	1.51
Current Density	A/mm^2	1	–	0.08	0.270	0.61	0.05
L/R_{DC}	nH/mΩ	2.85	14.57	0.731	0.422	0.277	14.02
Peak $Q^{\dagger}$		15	–	38	14.3	14.5	28
κ		5.1	–	–	$\approx$2.5	–	$\approx$2.4

Table 4.10: Comparison of properties with state of the art embedded inductors. This work considers IND048 with HPE1.

Property	Units	This work	Solenoid [11]	Toroid [21]	Solenoid [17]	Solenoid [17]
Area	mm^2	5	3.75	2.9	3.4	3.4
Thickness	μm	600	15	400	150	150
Material μ_r		185	600	5	–	–
Material Type		MPC	Thin-film	MnZn comp.	Bulk	Bulk
Turns		5	34	12	10.5	22
Switching Freq.	MHz	2	10	10	1	1
Inductance L	nH	480	158	43.6	297.9	1005.8
Inductance Density	nH/mm^2	96	42	15	87	295
DC Resistance	mΩ	22.8	1000	280	619	797
L/R_{DC}	nH/mΩ	21.1	0.158	0.156	0.481	1.26
Saturation Current	A	0.1	–	8	0.9	0.1
I_{DC} @ 150 mW	A	2.56	0.387	0.730	0.492	0.433

4.8 Summary

Several magnetic materials were uses to understand the behavior of the inductors and validate the design framework and performance metric r_{acx}. We used three low-frequency flake-filler metal polymer composite (MPC) magnetic materials with relative permeabilities 180, 75, and 45, and three high-frequency spherical-filler MPC magnetic materials with relative permeabilities 24, 9.1, and 7. A process was developed to fabricate the embedded inductors using a magnetic sheet with 400 μm thickness. In this process, slots are drilled in a magnetic sheet and then filled with a polymer. These slots ensure maximum coupling between vias and provide electrical isolation between the vias and the metal fillers. Then vias a drilled in the polymer. Using a lithography and electroplating process the top and bottom metal layers are patterned with the inductor layout. Several optimization steps, for the drilling and slots filling, were made to ensure every step worked as expected.

We showed the exploration results of 7 inductor designs, each with 6 different magnetic materials. The small signal spectra with and without DC bias was measured. The three materials targeted for low frequency applications showed a very low saturation current that makes them impossible to be used in power converters. On the other hand, we tested 3 high frequency materials with saturation over 5 A. However, the inductance with these high frequency materials is considerably lower. From these six materials, only HBS1 shows some amount of inductance with high current capability.

Using the small signal spectra, the r_{acx} values for all the inductors at different frequencies were compared. It is observed that it is invariant with respect to the amount of inductance and is characteristic of each material. This property allows its use as a benchmark metric to compare the small signal properties of different materials. It is also be observed that the materials losses increase drastically with duty cycles of less than 20%. This duty cycle dependency sets a constraint to the power stage topologies and creates the link for the co-design.

The large and small signal losses were compared using materials HPE2 and HBS1, showing that the large signal losses can be over 5 times larger. It was observed a relationship between the small and large signal losses, and this relationship allows to determine the conversion ratio space for a given material. From all the material, only HBS1 can be used at 10 MHz, where its optimum conversion ratio is 1.7 V to 1 V with maximum inductor efficiency of 95% and maximum output current of 5 A.

Reliability measurements, such as aging with respect to thermal cycles and time-of-use in a buck converter, must be covered in a future work.

When compared to the state of the art inductors, the inductor combination of IND048 with HBS1 present a higher L/R_{DC} ratio and a higher maximum current.

CHAPTER 5

SMALL SIGNAL SPICE CIRCUIT MODEL

In this Chapter, we explore a SPICE inductor model that follows a physical behavior insight, as opposed to models that use RLC ladder networks to fits the inductor response based on pole/zeros. Our model uses the knowledge on the inductor losses in the presence of magnetic materials. In Figure 5.1 the full 10-elements inductor model is presented.

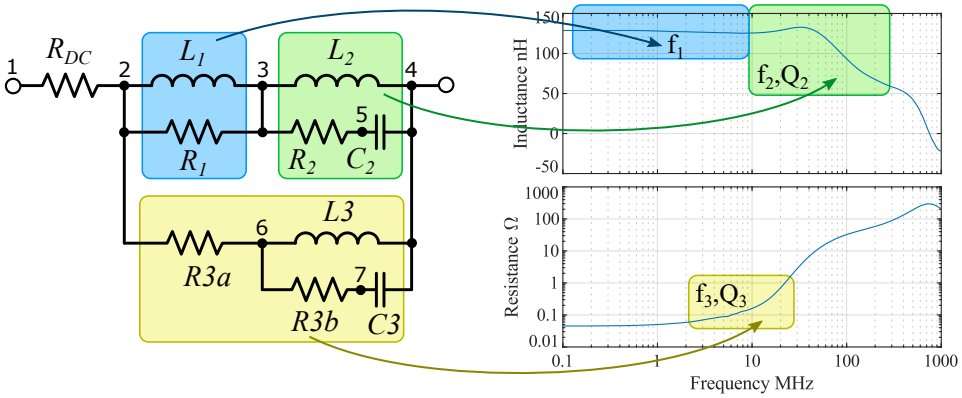


Figure 5.1: To the left the small signal full inductor model, called SM0. To the right the frequency response and model branches relationship.

In the model we can identify three main branches: i) branch 1 is used to model the DC and high frequency inductance variation, ii) branch 2 models the inductance change at the FMR frequency, iii) and branch 3 models the change of resistance slope at the FMR frequency. However, this model suffers from over-fitting, due to the interaction of all the circuit elements. This over-fitting also has a consequence that the optimization algorithm has many local minima, therefore, it is important to properly specify the initial conditions, which are defined as follow,

$$
\begin{aligned}
L_1 &= 0.5L \\
R_1 &= 2\pi\, f_1 L_1 \\
L_2 &= 0.5L \\
C_2 &= \frac{1}{(2\pi f_2)^2 L_2} \\
R_2 &= \frac{1}{2\pi f_2 Q_2 C_2} \\
R_{3a} &= 1 \\
R_{3b} &= \max(R_{AC}) \times 200 \\
L_3 &= \frac{1}{2\pi f_3 \times 10^{-3/2}} \\
C_3 &= \frac{1}{2\pi f_3 \times 10^{-3/2}}
\end{aligned}
$$

The error function used for the optimization problem and find the element values that best fit the inductor frequency response is shown in Listing 1. The error function first re-samples the small signal spectra in logarithm scale. In order to give to the inductance and resistance the same weight, both are normalized in the range of $[0.5\,1.5]$. Then, the RMS of the errors are added up together. Using Object-Oriented-Programming and polymorphism, the function `self.response()` change according to the programmed inductor model.

Two optimization methods are used. First, using particle swarm algorithm we try to find the global minima, and then using `fmincon` we refine the found minima. The optimization function is shown in Listing 2. Due to over-fitting, the optimization can result in some circuit elements with very high values, meaning those elements are discarded. This results in degenerated inductor circuit models. We can initially determine the sub-models as shown in Figure 5.2.

```
function err = error(self, x)
    % frequency range
    N = 100;
    fmin = self.inductor.f(1);
    fmax = self.inductor.f(end)/2;
    f = logspace(log10(fmin),log10(fmax),N);
    f(1) = fmin;
    f(end) = fmax;

    % Values from simulated or measured inductor
    [Lr,Rr] = self.inductor.at(f);
    % Values from the circuit model
    [Lm,Rm] = self.response(x,f);

    % Map the resistance to Log scale
    Rr = log10(Rr);
    Rm = log10(Rm);

    % Normalization to [0.5,1.5]
    L_min = min(Lr);
    L_max = max(Lr);
    L_en = (Lr - L_min)/(L_max - L_min) + 0.5;
    L_mn = (Lm - L_min)/(L_max - L_min) + 0.5;

    % Normalization to [0.5,1.5]
    R_min = min(Rr);
    R_max = max(Rr);
    R_en = (Rr - R_min) / (R_max - R_min) + 0.5;
    R_mn = (Rm - R_min) / (R_max - R_min) + 0.5;

    % Relative errors
    L_error = 1-L_mn./L_en;
    Rac_error = 1-R_mn./R_en;

    % Error function evaluation
    err = 0.5*sqrt(sum(L_error.^2)/(N-1)) + 1.5*sqrt(sum(Rac_error.^2)/(N-1));
end
```

Listing 1: MATLAB code for the Conjugate Gradient iterative solver.

```
function fit(self)
    % Vector with initial values
    x0 = self.initialCondictions();

    % Define the objective function
    objfun = @(x) self.error(x);

    % Find global minimum using particle swarm
    ps_options = optimoptions('particleswarm');
    ps_options.Display = 'iter';
    ps_options.SwarmSize = 100;
    ps_options.MaxIterations = 500;
    ps_options.InitialSwarmMatrix = repmat(x0,length(x0),1);

    x0 = particleswarm(objfun, length(x0), zeros(1,length(x0)), [], ps_options);

    % Refine using fmincon
    A = -eye(length(x0));
    b = zeros(length(x0),1);
    fm_options = optimoptions('fmincon');
    fm_options.Display = 'iter';
    fm_options.MaxIterations = 1000;

    self.x = fmincon(objfun,x0, A,b,[],[],[],[],[],fm_options);

    % Copy result from vector x to circuit elements RLC
    self.unpack();
end
```

Listing 2: MATLAB code for the Conjugate Gradient iterative solver.

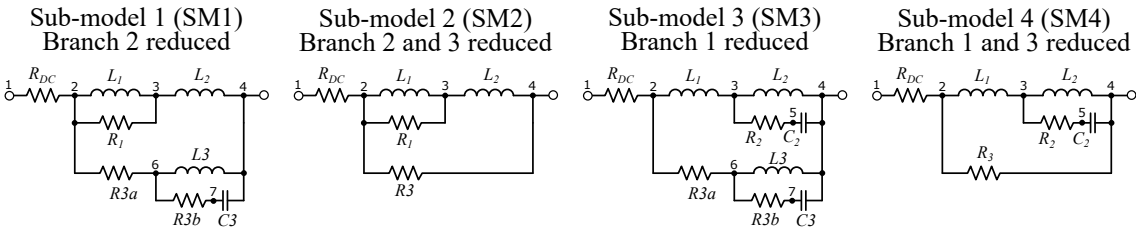


Figure 5.2: Inductor sub-models.

The advantage to use this physical behavior based models is that they can be easily scaled to model any amount of inductance. It is enough to properly model one inductor with a given material, to then using a scaling factor to predict the response of other inductors with different amount of inductance. If the scaling factor is ta, then resistors and inductors scale proportionally to ta and capacitors scale proportionally to $1/ta$. The inductors IND034, IND035, IND036, and IND037 with materials HPE2 and HBS1 are used as examples (material HPE1 and RM4A have a similar response compared to HPE2).

The inductor model will be fitted to IND034 with HPE2 and to IND035 with HBS1. In Figure 5.3 it is shown the result of the circuit model for both. As the figure shows, the circuit model matches very well with the measurements. The resulting circuit elements are shown in Figure 5.4.

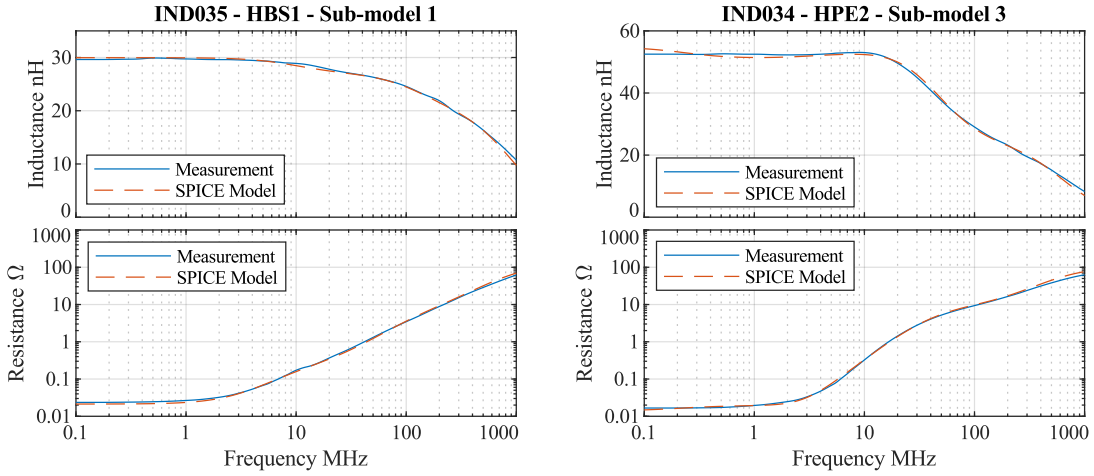


Figure 5.3: Inductor reference sub-model fitting.

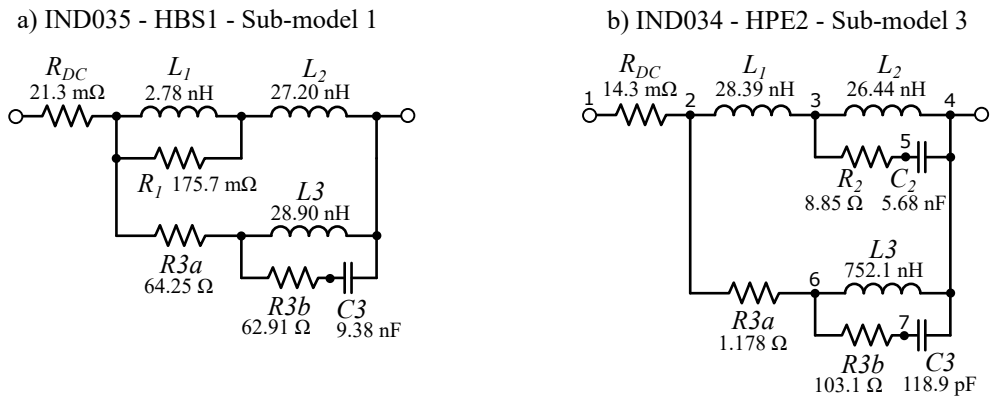


Figure 5.4: Inductor reference sub-model fitting.

Using these models as reference, we can now scale them to match the measurements of the rest of the inductor structures. In Figure 5.5 it is shown the comparison between measurements and the reference circuit model scaled by the factor ta. As it can be observed, the scaled models fit remarkably well the measurements.

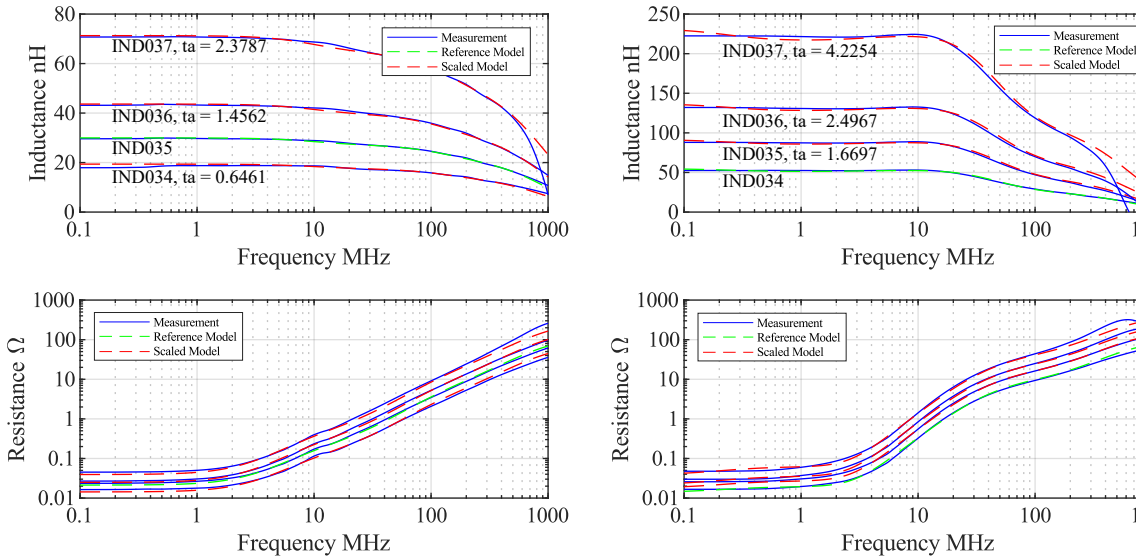


Figure 5.5: Inductor measurement and scaled sub-model comparison.

However, these models can only be used with small signal measurements. It cannot take into account for the loss factor κ. More work is required to refine the model to include the large signal losses.

5.1 Summary

The simple RL model used in the previous section is only useful for analysis and plotting, but not for circuit simulation. A SPICE model based on the inductor physical behavior and the optimization algorithm was presented. To properly fit the measured small-signal spectra, a normalization in logarithm scale is done for the inductance and resistance. This method sets the same weight to both inductance and resistance, and a more equalized weight with respect to its dimension and frequency.

Using the measurements and experimentation it was shown that with these models it is possible to obtain the inductance and resistance spectra of difference inductors with different amounts of inductance with excellent accuracy by just applying a scaling factor. However, this model only takes into account the small-signal losses. To include the total inductor losses, more work is needed to take into account the large to small losses factor κ.

CHAPTER 6

DESIGN AND POWER LOSS EXTRAPOLATION

In Chapter 4, it was shown that the Effective AC resistance per unit inductance is very insensitive, or invariant, to changes of geometry and the amount of inductance. In this Chapter, we explore this property by comparing the embedded inductor results with a simple discrete toroidal inductor, as shown in Figure 6.1, fabricated with materials HBS1, HPE1, and HPE2. Figure 6.2 shows the comparison of the small signal r_{acx} of this toroidal inductor (in dash green lines) with the embedded inductors in black lines).

HBS1, 400 um thickness ID: 3 mm, OD: 8 mm Turns = 10 R_{DC} = 21 mΩ L = 300 nH @ 2 MHz	HPE2, 400 um thickness ID: 3 mm, OD: 8 mm Turns = 10 R_{DC} = 21 mΩ L = 625 nH @ 2 MHz	HPE1, 200 um thickness ID: 3 mm, OD: 8 mm Turns = 10 R_{DC} = 21 mΩ L = 1450 nH @ 2 MHz	

Figure 6.1: Simple discrete toroidal inductor.

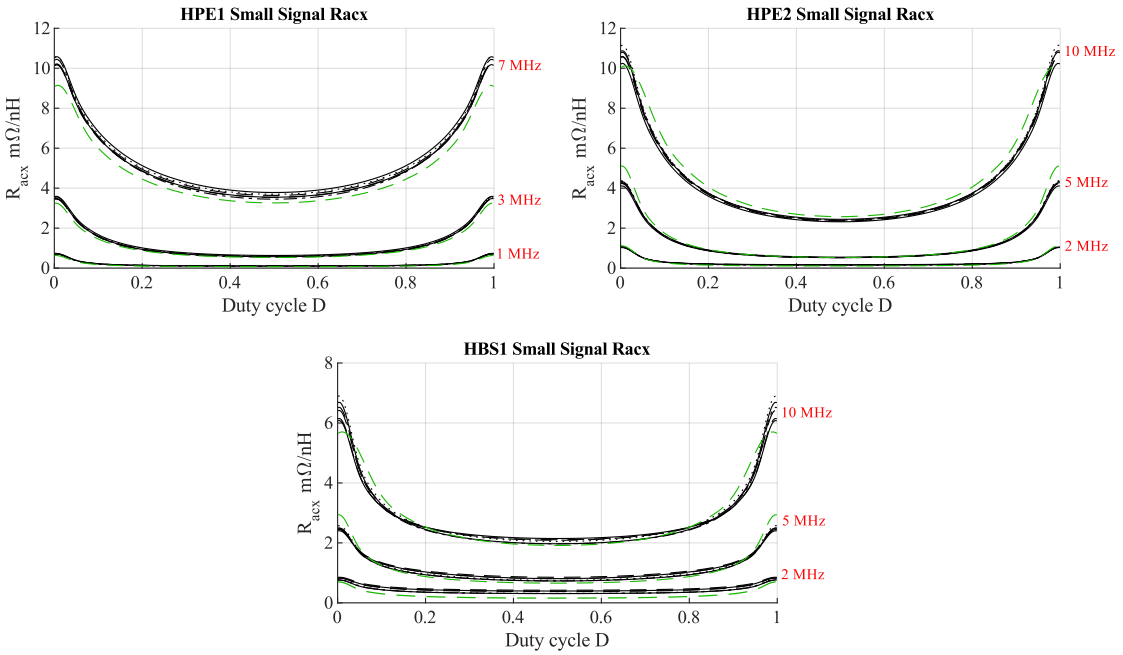


Figure 6.2: Simple discrete toroidal inductor r_{acx} (green dash line) comparison.

We observe that the r_{acx} values of the discrete toroidal inductor are very close to the result of the embedded ones. For materials HPE1 and HPE2, we note a higher value at higher frequencies, this is produce because the discrete toroidal inductor has a higher inter-winding capacitance which reduces the inductance and increases the losses at high frequencies. For HBS1, we note that the discrete toroid has a lower r_{acx} at lower frequencies. To understand this, in the expression (Equation 3.16) the term R_{AC}/L needs to be separated between the air core contribution for the inductance L_{air} and resistance R_{air} and the increment, due to the inclusion of the magnetic material, of the inductance ΔL_{mag} and resistance ΔR_{mag}. Let us use the subscript 1 in $L_{air,1}$, $\Delta L_{mag,1}$, and $\Delta R_{mag,1}$ to denote the values per turns N, then we have

$$\frac{R_{AC}}{L} = \frac{R_{air} + \Delta R_{mag}}{L_{air} + \Delta L_{mag}} = \frac{N\, R_{air,1} + N^2 \Delta R_{mag,1}}{N^2\, L_{air,1} + N^2\, \Delta L_{mag,1}} \tag{6.1}$$

The R_{air} is only proportional to the number of turns, as it is due to the copper resistance and the skin depth. The previous expression can be simplified to,

$$\frac{R_{AC}}{L} = \frac{\frac{R_{air,1}}{N} + \Delta R_{mag,1}}{L_{air,1} + \Delta L_{mag,1}} \tag{6.2}$$

therefore, with a larger number of turns or magnetic losses, the ratio R_{AC}/L becomes:

$$\frac{R_{AC}}{L} = \frac{\Delta R_{mag}}{L_{air} + \Delta L_{mag}} \tag{6.3}$$

then, when copper losses are comparable to magnetic losses, the r_{acx} will reduce slightly with an increase in the number of turns.

The results of the large signal current ripple sweep for the discrete toroidal inductor with material HBS1 are shown in Table 6.1. We obtained the same values for the R_{acx} and for the ratio R_{acx}/r_{acx}. In Table 6.2 it is shown the large signal frequency sweep results, and we see that the ratio between frequencies of 2 MHz to 5 MHz is also 5.8.

Table 6.1: Inductor IND037 - HBS1 parameters from large signal current ripple Δi_L sweep at $f_s = 5$ MHz. L_{sm} corresponds to the small signal inductance.

L_{sm}	nH	297	297	297	297	297	297	297	297
r_{acx}	$\frac{\text{m}\Omega}{\text{nH}}$	0.658	0.658	0.658	0.658	0.658	0.658	0.658	0.658
L	nH	294.7	297.6	299.4	298.4	305.6	303.2	304.2	306.7
Δi_L	mA	40.65	59.96	98.58	137.2	174.8	217.5	274.4	349.6
P_{AC}	mW	1.822	4.219	11.16	21.43	35.62	54.34	88.00	145.4
R_{acx}	$\frac{\text{m}\Omega}{\text{nH}}$	3.742	3.943	3.835	3.816	3.815	3.790	3.842	3.878
Ratio	$\frac{R_{acx}}{r_{acx}}$	5.690	5.997	5.831	5.803	5.802	5.763	5.842	5.897

Table 6.2: Inductor IND037 - HBS1 parameters from large signal frequency f_s sweep at $D = 0.5$. L_{sm} corresponds to the small signal inductance.

f_s		2	3	4	5
L_{sm}	nH	302.4	300.7	299.1	297.3
r_{acx}	$\frac{\text{m}\Omega}{\text{nH}}$	0.158	0.291	0.461	0.658
L	nH	307.5	304.8	301.3	297.9
Δi_L	mA	133.1	133.1	133.1	135.2
P_{AC}	mW	4.227	9.186	14.37	20.43
R_{acx}	$\frac{\text{m}\Omega}{\text{nH}}$	0.776	1.700	2.691	3.753
Ratio	$\frac{R_{acx}}{r_{acx}}$	4.910	5.850	5.837	5.707

In Figure 6.3 it is shown the large signal comparison of the discrete toroidal inductor with the embedded inductor IND037 at 5 MHz.

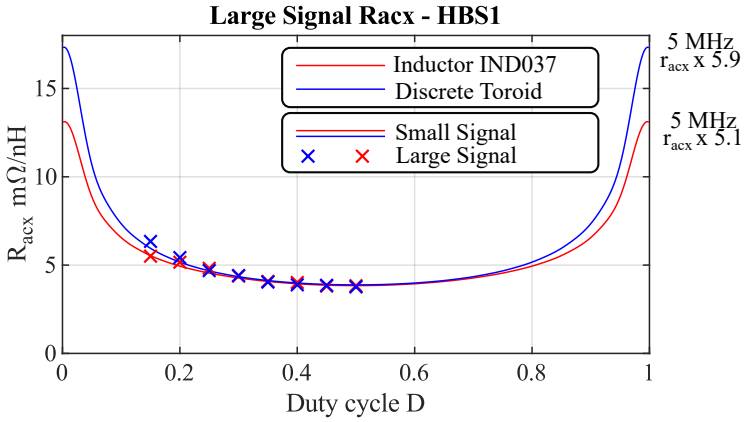


Figure 6.3: Large signal R_{acx} comparison between the discrete toroid and embedded inductor IND037.

Despite these minor differences, the discrete toroidal inductor can be used to predict the R_{acx} of more complex embedded structures. The fabrication of the discrete toroid takes only one day and is very inexpensive, in contrast to the embedded inductors that can take a few months. For material research, this saves a considerable amount of time. We believe this simple method, using the R_{acx} metric, will allow improved designs of inductors, magnetic materials, and IVRs to power the next generation of high-performance computing (HPC) platforms.

For the small signal spectra with DC bias current measurement, we used the discrete toroid with HBS1 and HPE2, but also it was fabricated with material HPE2 a discrete toroidal inductor with a 150 μm air gap, as shown in Figure 6.4;

Figure 6.4: Simple discrete toroidal inductor with 150 μm air-gap using material HPE2.

Figure 6.5 shows how the saturation current improves with the air-gap. However, we also observe that the saturation current reaches the same point of 1.25 A for both HPE1 and HPE2. Also, we observe that, the inductance of the HPE2 toroid with the air-gap get close to the inductance of the HBS1 toroid. Still, the HBS1 material has a saturation current over 5 A, thanks to its distributed air-gap material.

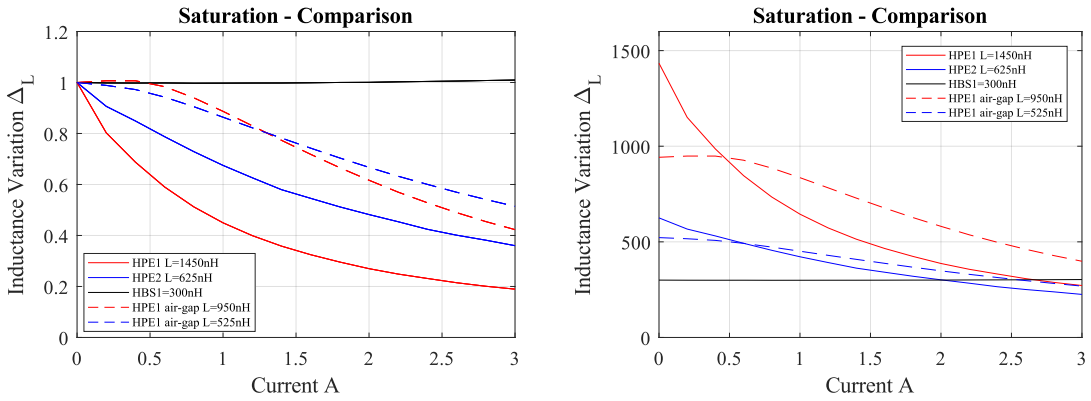


Figure 6.5: Comparison of saturation current between inductor with and without air-gap.

6.1 Roadmap for Future Magnetics for High Conversion Ratio IVRs

We have observed that the most critical component of the design is not the inductor structure itself, but the magnetic material properties.

The inductor geometry will affect the inductance density, where more inductance help to reduce the AC losses because of the inverse relation of the losses to the inductance,

$$P_{L,AC} = \frac{V^2(1-D)^2}{4Lf_s^2} R_{acx}(D, f_s)$$

However, not much can be done to increase the inductance if the saturation current is too low, as is the case with the three low-frequency and high-permeability materials HPE1, HPE2, and RM4A. On the other hand, high saturation materials, like HBS1, MUE1, and MUF1, tend to have very low permeability. In addition, high permeability implies lower saturation current.

Based on the analyzed materials, the ideal material may need to have a combination of the properties of these two different magnetic composites. The low-frequency high-permeability materials can achieve high inductance and very low small signal losses thanks to their flake filler, creating a micro lamination structure. The ultra low small-signal losses of RM4A indicate that the fillers must be coated to prevent bulk-conductivity. And, the distributed "air-gap" of the spherical fillers allows for a very high saturation current. We

believe that a hybrid flake-spherical bi-magnetic (combination of low and high permeability materials) coated filler metal composite can be the key to achieve the required magnetic properties. As was shown in the previous section, distributed air-gaps have advantages compared to lumped air-gap. Make gaps with around 20 μm in the substrate are difficult to achieve, adding complexity, time, and cost to the fabrication.

With the high inductance density of the inductor structure IND048, a material with relative permeability 45 can achieve 120 nH. Therefore, a material with a permeability of around 65 can achieve an inductance of 170 nH as required for 12 V to 1 V conversion ratio. A material with the low loss characteristic of RM4A but with high enough saturation current, a large to small power loss ratio of $\kappa = R_{acx}/r_{acx} = 4$, and an inductance of 170 nH, would give an inductor efficiency of 95% for 12 V to 1 V at 1.875 A, as shown in Figure 6.6. Note that in a two-phases series capacitor buck converter for 12 V to 1 V conversion, each phase is powered by 6 V, and Figure 6.6 shows 95% inductor efficiency with an input voltage of 6 V, or equivalently, a duty cycle of 0.19.

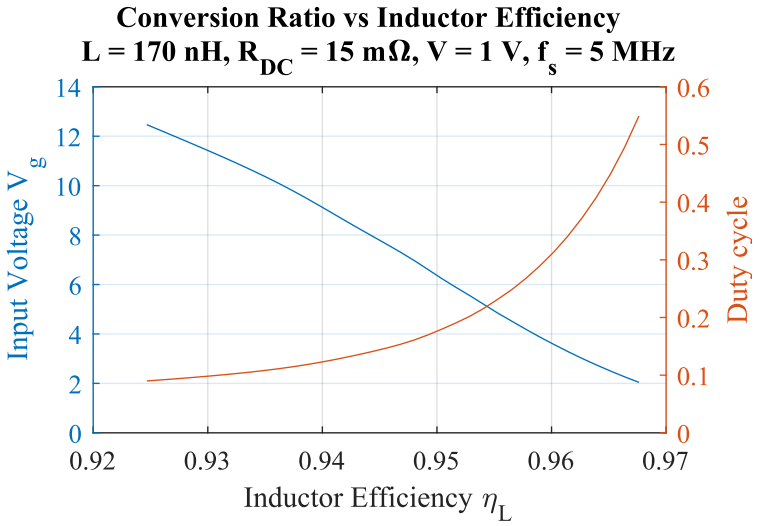


Figure 6.6: Conversion ratio space for required magnetic materials.

In Table 6.3 it is summarized the key properties of the target magnetic materials to make 12 V to 1 V conversion IVRs possible. For 48 V to 1 V the requirements are more tight and challenging, as shown in Table 6.4, where ultra low hysteresis losses must be achieved

(κ = 2.2) and the IVR power stage must have a switching frequency of 5 MHz.

Table 6.3: Key parameters for magnetic material for 12 V to 1 V conversion ratio IVR, at $f_s = 5$ MHz.

Parameters	Symbol	Units	Value
FMR	f_{FMR}	MHz	25
Permeability	μ'	-	65
Loss tangent	$\tan\delta$	-	0.012
Saturation	H_{sat}	kA/m	>6
Loss ratio	κ	-	4
Large Signal	R_{acx}	mΩ/nH	1.208

Table 6.4: Key parameters for magnetic material for 48 V to 1 V conversion ratio IVR, at $f_s = 5$ MHz.

Parameters	Symbol	Units	Value
FMR	f_{FMR}	MHz	25
Permeability	μ'	-	75
Loss tangent	$\tan\delta$	-	0.012
Saturation	H_{sat}	kA/m	>6
Loss ratio	κ	-	2.2
Large Signal	R_{acx}	mΩ/nH	1.079

6.2 Summary

Expanding in the invariance property of the r_{acx} metric, we have shown the inductor losses and the R_{acx} of a simple discrete toroidal inductor, and how it compares against the results of the more complex embedded ones. We have shown that using the R_{acx} metric we can use a simple toroidal inductor to accurately predict the losses of more complex embedded inductor structures. This saves a considerable amount of time and resources allowing faster iterations for magnetic material research.

Using the same discrete toroidal inductors, it is shown that a lumped air-gap can be used to increase the saturation current for the low-frequency materials. However, its per-

formance is lower compared to the properties of spherical filler materials like the HBS1. This concluded that magnetic materials with engineered distributed air-gap are required.

Finally, using all the experimental results and the validated ideas and design framework, we have determined the required properties for a material, that when use with IND048 structure, provides the required inductance and efficiency to make a 12 V to 1 V IVR possible with a 95% of inductor efficiency. Such properties are a $f_{FMR} > 25$ MHz, relative permeability $\mu' = 65$, loss tangent $\tan\delta = 0.012$, saturation field $H_{sat} > 6$ kA/m, loss ratio $\kappa = 4$, and large signal $R_{acx} = 1.2$ mΩ/nH.

CHAPTER 7
CONCLUSION

Processors (CPU) and System on Chips (SoC) are increasing their performance and integration density (numbers of transistors and computational cores per IC) at the expense of higher power consumption. This increase in power requirement is translated to a higher package input current, which will not be possible to sustain with typical input voltages of 1.7 V. To solve this power delivery issue, higher input voltages, like 5, 12, or even 48 V, are considered as the solution for next generation SoCs for high performance computing platforms (HPCs). However, this high conversion ratio voltage regulators sets several challenges to Integrated Voltage Regulators (IVRs).

In this thesis we address the tasks of i) study the power loss breakdown of power converters to identify the components and factors with the highest impact on the system efficiency, ii) study the requirements for an inductor to be embedded, iii) propose a new inductor metric that includes the duty cycle allowing a co-design between the power stage and the inductor, iv) design a set of embedded inductors and its fabrication process to study the different properties of a set of magnetic materials, v) with measurements determine the usable space, or conversion ratio space, for the magnetic materials and determine what should be the properties of new materials to make high conversion IVRs possible.

The main power loss contributions come from the MOSFET switching losses given by the output capacitance and gate charge, and by the inductor DC and AC losses. To reduce the MOSFET losses, topologies like the hybrid series capacitor buck converter are used, with the additional benefit of a duty cycle extension. This extension in the duty cycle becomes a requirement to reduce the inductor AC losses.

Regardless of the power stage topology, embedded inductors are place between conduction planes, usually ground and power, and this set constraints to their structure. Only

an inductor that has a close magnetic path (all the magnetic field is contained in a magnetic material) can be embedded without affecting its performance. Using magnetic sheets and through vias it is possible to fabricate solenoids or toroids with a close magnetic path, opening the possible inductor geometries.

Using six different magnetic sheets, seven inductor designs were fabricated. These inductors have inductances ranging from 20 nH to 500 nH, DC resistances between 14 mΩ and 40 mΩ, and saturation currents from 100 mA to over 5 A. Using the proposed inductor performance metric called Effective AC resistance per unit inductance, or R_{acx}, it was shown that this metric is mostly invariant with the inductor structure and amount of inductance. This allows to determine the inductor properties based on the inductor efficiency as the objective function, to then find the inductor structure that can achieve the calculated inductance and DC resistance. Three of the analyzed magnetic materials have high permeability, flake fillers, and are targeted for low frequency applications. However, these three magnetic sheets have a saturation current of less than 100 mA making them unsuitable for power applications. The other three magnetic sheets have low permeability, spherical fillers, and are targeted to high frequency converters. With these three high frequency materials, all the inductor designs show saturation currents over 5 A, however, the amount of inductance is not enough.

It was found that the large signal losses are related by a factor to the small signal losses. Using the r_{acx} metric, it is very easy to determine the small signal losses. To find the total losses it is only required to multiply the r_{acx} by the loss ratio constant κ. With all this information, based on analytical results, simulation, and measurements, it is possible to determine the properties that new magnetic materials must have in order to make high conversion ratio IVRs possible.

The invariance property of the R_{acx} metric was validated even with a drastically different discrete toroidal inductor. This allows advancing the research of magnetic materials and inductor performance at an increased pace. Discrete toroidal inductors can take a sin-

gle day of work, compared to several months for novel embedded inductors. This opens the door for more and faster magnetic material research iterations.

Finally, using all the experimental results and the validated ideas and design framework, we have determined the required properties for a material, that when used with IND048 structure, provides the required inductance and efficiency to make a 12 V to 1 V IVR possible with a 95% of inductor efficiency. Such properties are a $f_{FMR} > 25$ MHz, relative permeability $\mu' = 65$, loss tangent $\tan\delta = 0.012$, saturation field $H_{sat} > 6$ kA/m, loss ratio $\kappa = 4$, and large signal $R_{acx} = 1.2$ mΩ/nH.

Appendices

APPENDIX A

INDUCTOR CURRENT SINE FOURIER EXPANSION

Figure Figure A.1 shows the inductor current waveform, where Δi_L is the ac ripple amplitude.

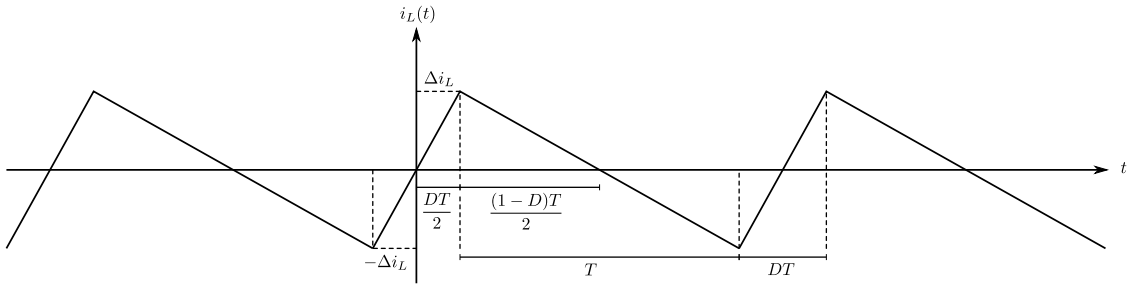


Figure A.1: Inductor current waveform.

The ripple current can be defined as a piecewise function $i_L(t)$

$$i_L(t) = \begin{cases} \frac{2\,\Delta i_L}{DT} t & 0 \leq t < \frac{DT}{2} \\ \frac{\Delta i_L}{1-D}\left(1 - \frac{2t}{T}\right) & \frac{DT}{2} < t < \frac{T}{2} \end{cases}$$

and can be represented with a sine Fourier expansion has the form,

$$i_L(t) = \sum_{n=1}^{\infty} b_n \, \sin\left(\frac{2n\pi}{T} t\right) \tag{A.1}$$

where the b_n coefficients are calculated as follow,

$$b_n = \frac{2}{T/2} \int_0^{\frac{T}{2}} i_L(t) \, \sin\left(\frac{2n\pi}{T} t\right) dt \tag{A.2}$$

and caring on the calculation,

$$b_n = \frac{4}{T}\int_0^{\frac{DT}{2}} \frac{2\Delta i_L}{DT} t\ \sin\left(\frac{2n\pi}{T}t\right) dt + \frac{4}{T}\int_{\frac{DT}{2}}^{\frac{T}{2}} \frac{\Delta i_L}{1-D}\left(1-\frac{2t}{T}\right)\sin\left(\frac{2n\pi}{T}t\right) dt$$

$$b_n = \frac{8\Delta i_L}{DT^2}\int_0^{\frac{DT}{2}} t\ \sin\left(\frac{2n\pi}{T}t\right) dt - \frac{8\Delta i_L}{(1-D)T^2}\int_{\frac{DT}{2}}^{\frac{T}{2}} t\ \sin\left(\frac{2n\pi}{T}t\right) dt$$
$$+ \frac{4\Delta i_L}{(1-D)T}\int_{\frac{DT}{2}}^{\frac{T}{2}} \sin\left(\frac{2n\pi}{T}t\right) dt$$

Using integration by parts,

$$u = t \qquad du = dt$$
$$dv = \sin\left(\frac{2n\pi}{T}t\right) \qquad v = \frac{-T}{2n\pi}\cos\left(\frac{2n\pi}{T}t\right)$$

$$b_n = \frac{8\Delta i_L}{DT^2}\left[\frac{-Tt}{2n\pi}\cos\left(\frac{2n\pi}{T}t\right)\Big|_0^{\frac{DT}{2}} + \frac{T}{2n\pi}\int_0^{\frac{DT}{2}} \cos\left(\frac{2n\pi}{T}t\right) dt\right]$$
$$- \frac{8\Delta i_L}{(1-D)T^2}\left[\frac{-Tt}{2n\pi}\cos\left(\frac{2n\pi}{T}t\right)\Big|_{\frac{DT}{2}}^{\frac{T}{2}} + \frac{T}{2n\pi}\int_{\frac{DT}{2}}^{\frac{T}{2}} \cos\left(\frac{2n\pi}{T}t\right) dt\right]$$
$$+ \frac{4\Delta i_L}{(1-D)T}\frac{-T}{2n\pi}\cos\left(\frac{2n\pi}{T}t\right)\Big|_{\frac{DT}{2}}^{\frac{T}{2}}$$

$$b_n = \frac{8\Delta i_L}{DT^2}\left[\frac{-T^2 D}{4n\pi}\cos(n\pi D) + \frac{T^2}{4n^2\pi^2}\sin\left(\frac{2n\pi}{T}t\right)\Big|_0^{\frac{DT}{2}}\right]$$
$$- \frac{8\Delta i_L}{(1-D)T^2}\left[\frac{-T^2}{4n\pi}\cos(n\pi) + \frac{T^2 D}{4n\pi}\cos(n\pi D) + \frac{T^2}{4n^2\pi^2}\sin\left(\frac{2n\pi}{T}t\right)\Big|_{\frac{DT}{2}}^{\frac{T}{2}}\right]$$
$$- \frac{2\Delta i_L}{(1-D)n\pi}[\cos(n\pi) - \cos(n\pi D)]$$

$$b_n = \frac{2\Delta i_L}{D}\left[\frac{-D}{n\pi}\cos(n\pi D) + \frac{1}{n^2\pi^2}\sin(n\pi D)\right]$$
$$- \frac{2\Delta i_L}{1-D}\left[\frac{-1}{n\pi}\cos(n\pi) + \frac{D}{n\pi}\cos(n\pi D) - \frac{1}{n^2\pi^2}\sin(n\pi D)\right]$$
$$- \frac{2\Delta i_L}{(1-D)n\pi}[\cos(n\pi) - \cos(n\pi D)]$$

$$b_n = \frac{2\Delta i_L}{n\pi}\left(-1 - \frac{D}{1-D} + \frac{1}{1-D}\right)\cos(n\pi D) + \frac{2\Delta i_L}{n^2\pi^2}\left(\frac{1}{D} + \frac{1}{1-d}\right)\sin(n\pi D)$$

$$b_n = \frac{2\Delta i_L}{D(1-D)} \cdot \frac{\sin(n\pi D)}{n^2\pi^2} \tag{A.3}$$

Finally we have for $i_L(t)$,

$$i_L(t) = \frac{2\Delta i_L}{D(1-D)} \sum_{n=1}^{\infty} \frac{\sin(n\pi D)}{n^2\pi^2} \sin\left(\frac{2n\pi}{T}t\right) \tag{A.4}$$

APPENDIX B

AC INDUCTOR POWER LOSS

We can use the result for the sine Fourier expansion of $i_L(t)$ to find an expression for the power loss due to *ac* current on the inductor *ac* resistance.

The average inductor power loss is,

$$P_{L,avg} = \frac{1}{T}\int_0^T i_L(t)\, v_L(t)\, dt$$

Replacing (Equation A.4) in the previous equation we get.

$$P_L = \frac{4\Delta i_L^2}{D^2(1-D)^2}\frac{1}{T}\int_0^T \sum_{n=0}^{\infty}\frac{\sin(n\pi D)}{n^2\pi^2}\sin\left(\frac{2n\pi}{T}t\right)\cdot\sum_{m=0}^{\infty}\frac{\sin(m\pi D)}{m^2\pi^2}\sin\left(\frac{2m\pi}{T}t\right) R_{L,ca}(mf_s)\, dt$$

but the sin() functions are orthogonal and the integral of cross product vanished,

$$\int_0^T \sin(mx)\ \sin(nx)\, dx = 0 \quad \text{if} \quad m \neq n$$

then the expression for $P_{L,avg}$ is reduce to,

$$\begin{aligned} P_{L,avg} &= \frac{4\Delta i_L^2}{D^2(1-D)^2}\sum_{n=0}^{\infty}\frac{\sin^2(n\pi D)}{n^4\pi^4}R_{L,ca}(mf_s)\ \frac{1}{T}\int_0^T \sin^2\left(\frac{2n\pi}{T}t\right) dt \\ &= \frac{4\Delta i_L^2}{D^2(1-D)^2}\sum_{n=0}^{\infty}\frac{\sin^2(n\pi D)}{n^4\pi^4}R_{L,ac}(nf_s)\ \frac{1}{T}\int_0^T \left(\frac{1}{2}-\cos\left(\frac{2n\pi}{T}t\right)\right) dt \end{aligned}$$

to finally obtain the ac inductor power loss

$$P_{L,ac} = \frac{2\Delta i_L^2}{D^2(1-D)^2}\sum_{n=0}^{\infty}\frac{\sin^2(n\pi D)}{n^4\pi^4}R_{L,ac}(n\, f_s) = \sum_{n=0}^{\infty}\frac{b_n^2}{2}R_{L,ac}(n\, f_s) \qquad \text{(B.1)}$$

APPENDIX C

MOSFET POWER LOSS TRANSITIONS

All the MOSFET switching transitions are shown in Figure C.1, with the power loss timing drawn in gray.

C.0.1 Gate Charge Losses

The gate charge losses is given by [53]

$$P_G = Q_G \, V_{GDR} \, f_s = C_{iss}^2 \, V_{GDR}^2 \, f_s \tag{C.1}$$

where $Q_G = Q_{GS1} + Q_{GS2} + Q_{GD} + Q_{ODRV}$ is the total gate charge,

The charge Q_{GS1} is given by,

$$Q_{GS1} = \frac{Q_{GS}}{V_{pl}} \, V_{th} \tag{C.2}$$

where Q_{GS} is the gate charge given in the datasheet at a specific I_{DS} and V_{DS}, V_{pl} is the gate plateau voltage taken from the I_{DS} vs V_{GS} plot at the given current for Q_{GS}.

Q_{GS2} can be calculated with,

$$Q_{GS2} = \frac{Q_{GS}}{V_{pl}} \, V_{pl(op)} - Q_{GS1} \tag{C.3}$$

where $V_{pl(op)}$ is the plateau voltage at the operational current.

The Miller charge Q_{GD} (only for the HS switch) can be calculated from the C_{rss} capacitance curve as follow,

$$Q_{GD} = \int_0^{V_g} C_{rss}(v_{_{DS}}) dv_{_{DS}} \tag{C.4}$$

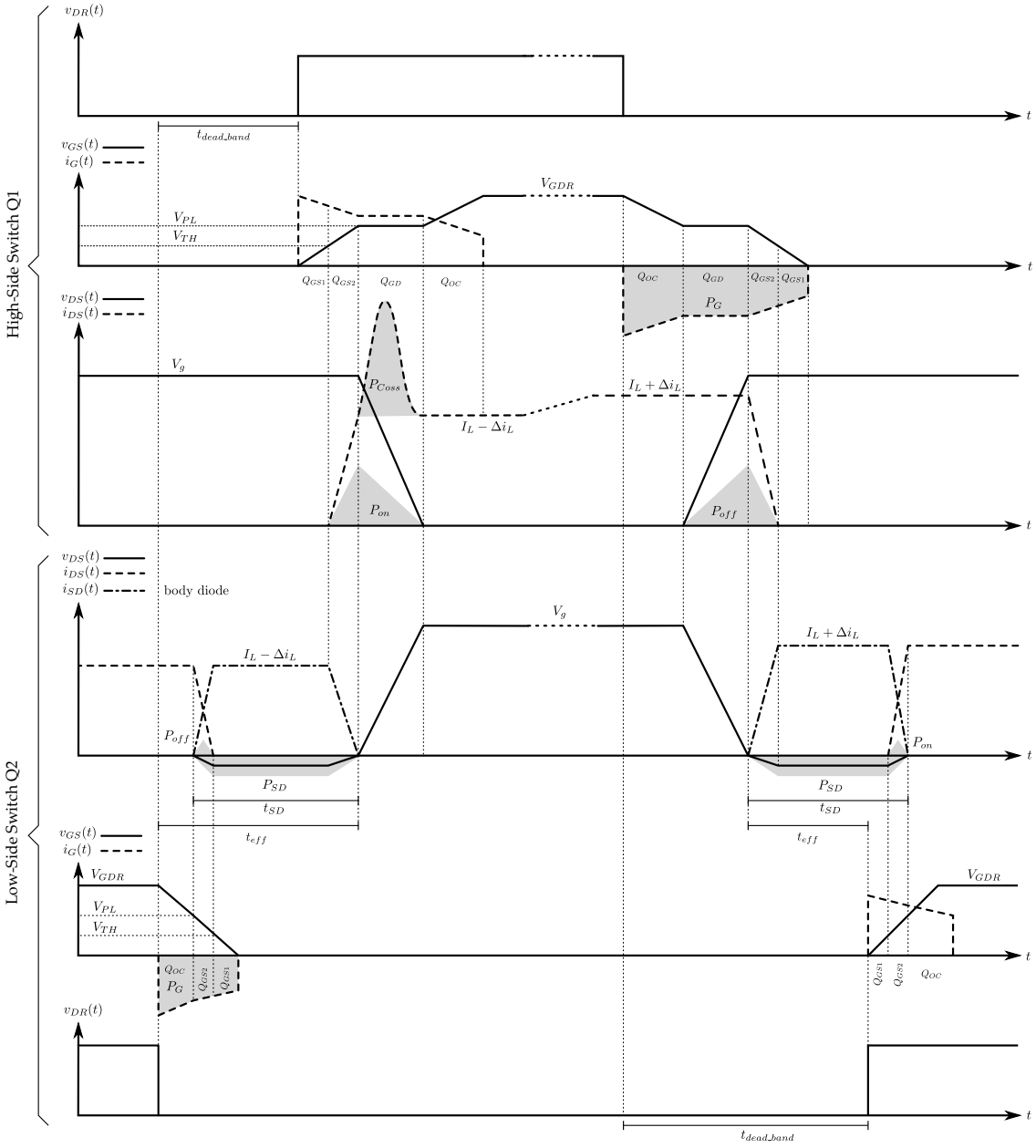


Figure C.1: GaN dynamic waveforms.

Finally, Q_{ODRV} can be calculated using the slope of the curve V_{GS} vs Q_G, this slope is independent of the working current or voltage.

$$Q_{ODRV} = m_{QG} \cdot (V_{DRV} - V_{pl}) \tag{C.5}$$

C.0.2 Turn-on and Turn-off Losses P_{IV}

Then the Turn-on and Turn-off Losses P_{IV} for both high-side and low-side switches, as given in [53], is defined as,

$$P_{IV} = P_{HS,on} + P_{HS,off} + P_{LS,on} + P_{LS,off} \tag{C.6}$$

$$P_{HS,on} = \frac{1}{2} V_g \left(I_L - \Delta i_L\right) \left(\frac{Q_{GS2}}{I_{Gon,1}} + \frac{Q_{GD}}{I_{Gon,2}}\right) f_s \tag{C.7}$$

$$P_{HS,off} = \frac{1}{2} V_g \left(I_L + \Delta i_L\right) \left(\frac{Q_{GD}}{I_{Goff,1}} + \frac{Q_{GS2}}{I_{Goff,2}}\right) f_s \tag{C.8}$$

$$P_{LS,off} = \frac{1}{2} V_{SD} \left(I_L - \Delta i_L\right) \left(\frac{Q_{GD}}{I_{Goff,1}} + \frac{Q_{GS2}}{I_{Goff,2}}\right) f_s \tag{C.9}$$

$$P_{LS,on} = \frac{1}{2} V_{SD} \left(I_L + \Delta i_L\right) \left(\frac{Q_{GS2}}{I_{Gon,1}} + \frac{Q_{GD}}{I_{Gon,2}}\right) f_s \tag{C.10}$$

and are produced because in the transition from on-state to off-state, or vice versa, the voltage and current are both non-zero across the MOSFET.

The gate currents depend on the gate driving circuit. If we assume a simple resistor R_G limiting current scheme, the gate currents are given by,

$$I_{Gon,1} = \left(V_{GDRV} - \frac{V_{PL} + V_{TH}}{2}\right) \frac{1}{R_{Gon}} \tag{C.11}$$

$$I_{Gon,2} = \frac{V_{GDRV} - V_{PL}}{R_{Gon}} \tag{C.12}$$

$$I_{Goff,1} = \frac{V_{PL}}{R_{Goff}} \tag{C.13}$$

$$I_{Goff,2} = \frac{V_{PL} + V_{TH}}{2R_{Goff}} \tag{C.14}$$

C.0.3 Output Capacitance Losses P_{oss}

The high-side and low-side *Output Capacitance Losses* is as follow,

$$P'_{Coss} = \int_0^{V_g} v_{DS}\, C_{oss}(v_{DS})\, dv_{DS} \cdot f_s \tag{C.15}$$

$$P_{Coss} = P'_{Coss,HS} + P'_{Coss,LS} \tag{C.16}$$

C.0.4 Reverse Conduction Losses P_{SD}

The low-side switch *Reverse Conduction Losses* is given by,

$$P_{SD} = V_{SD} \left(I_L \pm \Delta i_L \right) \, t_{SD} \, f_s \tag{C.17}$$

and has to be considered during the intervals Q_2 turn-off Q_1 turn-on, and Q_2 turn-on Q_1 turn-off.

APPENDIX D

POWER LOSS AND DUTY CYCLE ACCURACY EXAMPLE

As will be shown later, an accurate value for the duty cycle is required to predict the inductor losses. We use the GaN model presented previously to predict the switching losses and efficiency factor η_e. Table D.1 shows the conversion parameters used in this analysis, along with the predicted buck converter duty cycle D and efficiency η.

Table D.1: Parameters to compute the required R_{acx} as function of Inductance L. D_{DC} is the calculate duty cycle without the factor $1/\eta_e$, while D_{dyn} is the calculated duty cycle including the dynamic MOSFET losses.

Parameter	For 48 V to 1V	For 12 V to 1V
Target η_L	95%	
Target f_s	5 MHz	
Target V	1 V	
I_M per-phase	1.875 A	
P_L	98.7 mW	
R_{DC}	14 mΩ	
V_{DS}	12 V	6 V
Q_{HS}	EPC2203	EPC2007C
Q_{LS}	EPC2040	EPC2014C
D_{DC}	8.50 %	17.60 %
D_{dyn}	9.25 %	18.34 %
η	77.75 %	83.98 %

The analytical results, shown in Table D.1, are compared with a SPICE simulation using the GaN device models provided by the manufacturer. The simulated SPICE circuit is shown in Figure D.1, which corresponds to a two-phases series capacitor buck converter [32].

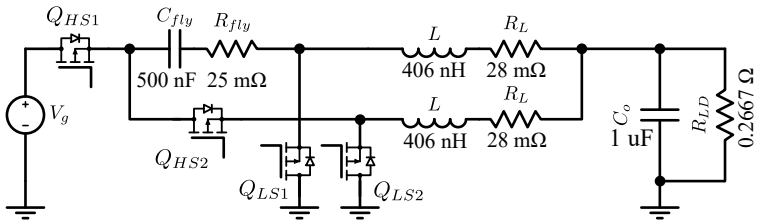


Figure D.1: SPICE circuit to compare with the duty cycle estimation using the analytical model of GaN and inductor.

Table D.2 shows the SPICE simulation results. The system efficiency η includes the losses of MOSFET output capacitance, gate charge, on-resistance, current-voltage overlap, and reverse conduction; and flying capacitor and inductor equivalent series resistance. For 48 V to 1 V we consider the converter with a duty cycle extension of 4 times (using a 2-phase series capacitor with half the input voltage, i.e. 24 V, which is equivalent to 4-phase series capacitor with the full input voltage, i.e. 48 V), and for 12 V to 1 V we consider a duty cycle extension of 2 times (using a 2-phase series capacitor).

Table D.2: Output voltage and efficiency result with SPICE simulation.

Parameter	For 48 V to 1V	For 12 V to 1V
D	9.25 %	18.34 %
V	1.0328 V	1.007 V
η	77.80 %	86.06 %

The analytical power loss calculations can predict very well the system losses and the duty cycle, where an accurate duty cycle value is important for quantification of the inductor losses.

REFERENCES

[1] S. Mappus, "Power converter topology trends," PSMA 2015 Power Technology Roadmap Presentations, 2014.

[2] C. Fei, M. H. Ahmed, F. C. Lee, and Q. Li, "Dynamic bus voltage control for light load efficiency improvement of two-stage voltage regulator," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–8.

[3] E. A. Burton *et al.*, "Fivr — fully integrated voltage regulators on 4th generation intel® core™ socs," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, pp. 432–439.

[4] H. M. Torun *et al.*, "Design space exploration of power delivery in heterogeneous integration," in *GOMACTECH*, 2019.

[5] S. Govindan and S. Venkataraman, "Silicon-package power delivery co-simulation with fully integrated voltage regulators on microprocessors," in *2014 IEEE Electrical Design of Advanced Packaging Systems Symposium (EDAPS)*, 2014, pp. 113–116.

[6] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2ed. Springer, 2001.

[7] J. Li, T. Abdallah, and C. Sullivan, "Improved calculation of core loss with nonsinusoidal waveforms," in *Conference Record of the 2001 IEEE Industry Applications Conference. 36th IAS Annual Meeting (Cat. No.01CH37248)*, vol. 4, 2001, 2203–2210 vol.4.

[8] S. Yue, Y. Li, Q. Yang, X. Yu, and C. Zhang, "Comparative analysis of core loss calculation methods for magnetic materials under nonsinusoidal excitations," *IEEE Transactions on Magnetics*, vol. 54, no. 11, pp. 1–5, 2018.

[9] J. Pries, L. Tang, and T. Burress, "Continuum modeling of inductor hysteresis and eddy current loss effects in resonant circuits," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 425–432.

[10] A. Elsherbini, H. Braunisch, K. O'Brien, and M. J. Hill, "Circuit modeling of nonlinear lossy frequency-dependent thin-film magnetic inductors," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 4, no. 1, pp. 145–152, 2014.

[11] J. M. Wright, D. W. Lee, A. Mohan, A. Papou, P. Smeys, and S. X. Wang, "Analysis of integrated solenoid inductor with closed magnetic core," *IEEE Transactions on Magnetics*, vol. 46, no. 6, pp. 2387–2390, 2010.

[12] P. R. Morrow, C. Park, H. W. Koertzen, and J. T. DiBene, "Design and fabrication of on-chip coupled inductors integrated with magnetic material for voltage regulators," *IEEE Transactions on Magnetics*, vol. 47, no. 6, pp. 1678–1686, 2011.

[13] N. Sturcken *et al.*, "A 2.5d integrated voltage regulator using coupled-magnetic-core inductors on silicon interposer delivering 10.8a/mm2," in *2012 IEEE International Solid-State Circuits Conference*, 2012, pp. 400–402.

[14] N. Sturcken, R. Davies, C. Cheng, W. E. Bailey, and K. L. Shepard, "Design of coupled power inductors with crossed anisotropy magnetic core for integrated power conversion," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2012, pp. 417–423.

[15] S. S. Boon, D. H. S. Wee, R. Salahuddin, and R. P. Singh, "Magnetic inductor integration in fo-wlp using rdl-first approach," in *2019 IEEE 21st Electronics Packaging Technology Conference (EPTC)*, 2019, pp. 18–22.

[16] M. S. Lekas, R. Davies, and N. Sturcken, "Magnetic thin-film inductors with induced radial anisotropy for improved inductance density," *IEEE Magnetics Letters*, vol. 10, pp. 1–4, 2019.

[17] Y. Hsieh, S. Lin, C. Kung, P. Lee, and C. Wang, "Ultra low profile power inductor integrated in wafer level package," in *2019 IEEE 21st Electronics Packaging Technology Conference (EPTC)*, 2019, pp. 175–178.

[18] Y. Dou, Z. Ouyang, P. Thummala, and M. A. E. Andersen, "Pcb embedded inductor for high-frequency zvs sepic converter," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 98–104.

[19] R. Murphy, Z. Pavlovic, P. McCloskey, C. O Mathuna, S. O'Driscoll, and G. Weidinger, "Pcb embedded toroidal inductor for 2mhz point-of-load converter," in *CIPS 2020; 11th International Conference on Integrated Power Electronics Systems*, 2020, pp. 1–5.

[20] R. Wu and J. K. Sin, "Novel silicon-embedded coreless coupled inductors for high efficiency on-chip dc-dc conversion," in *2011 IEEE Energy Conversion Congress and Exposition*, 2011, pp. 1827–1831.

[21] X. Fang, R. Wu, L. Peng, and J. K. O. Sin, "A novel silicon-embedded toroidal power inductor with magnetic core," *IEEE Electron Device Letters*, vol. 34, no. 2, pp. 292–294, 2013.

[22] W. J. Lambert, M. J. Hill, K. Radhakrishnan, L. Wojewoda, and A. E. Augustine, "Package inductors for intel fully integrated voltage regulators," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 6, no. 1, pp. 3–11, 2016.

[23] S. Muller, M. L. F. Bellaredj, A. K. Davis, P. A. Kohl, and M. Swaminathan, "Design exploration of package-embedded inductors for high-efficiency integrated voltage regulators," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 9, no. 1, pp. 96–106, 2019.

[24] T. Fukuoka *et al.*, "An 86% efficiency, 20mhz, 3d-integrated buck converter with magnetic core inductor embedded in interposer fabricated by epoxy/magnetic-filler composite build-up sheet," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 1561–1566.

[25] H. T. Le *et al.*, "High-q three-dimensional microfabricated magnetic-core toroidal inductors for power supplies in package," *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 74–85, 2019.

[26] C. Chiang *et al.*, "Embedded power inductor in organic substrate with novel magnetic epoxy," in *2020 IEEE 70th Electronic Components and Technology Conference (ECTC)*, 2020, pp. 1566–1572.

[27] X. Sun *et al.*, "3d heterogeneous package integration of air magnetic core inductor: 89% - efficiency buck converter with backside power delivery network," in *2020 Symposia on VLSI Technology and Circuits*, 2020.

[28] T. Sun *et al.*, "Substrate-embedded low-resistance solenoid inductors for integrated voltage regulators," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 10, no. 1, pp. 134–141, 2020.

[29] M. Sankarasubramanian *et al.*, "Magnetic inductor arrays for intel® fully integrated voltage regulator (fivr) on 10th generation intel® core™ socs," in *2020 IEEE 70th Electronic Components and Technology Conference (ECTC)*, 2020, pp. 399–404.

[30] C. Mathúna, N. Wang, S. Kulkarni, and S. Roy, "Review of integrated magnetics for power supply on chip (pwrsoc)," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4799–4816, 2012.

[31] K. Hirmer, K. Hofmann, T. Casper, and S. Schöps, "3d field simulation model for bond wire on-chip inductors validated by measurements," in *2019 Kleinheubach Conference*, 2019, pp. 1–4.

[32] Yungtaek Jang, M. M. Jovanovic, and Y. Panov, "Multiphase buck converters with extended duty cycle," in *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC '06.*, 2006, 7 pp.–.

[33] X. Zhao, C. Yeh, L. Zhang, J. Lai, and T. Labella, "A 2-mhz wide-input hybrid resonant converter with ultracompact planar coupled inductor for low-power integrated on-chip applications," *IEEE Transactions on Industry Applications*, vol. 54, no. 1, pp. 376–387, 2018.

[34] K. I. Hwu, W. Z. Jiang, and P. Y. Wu, "An expandable two-phase interleaved ultrahigh step-down converter with automatic current balance," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9223–9237, 2017.

[35] F. Marvi, E. Adib, and H. Farzanehfard, "Efficient zvs synchronous buck converter with extended duty cycle and low-current ripple," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 9, pp. 5403–5409, 2016.

[36] S. Mueller *et al.*, "Design of high efficiency integrated voltage regulators with embedded magnetic core inductors," in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, 2016, pp. 566–573.

[37] C. Chen *et al.*, "Ultra-low-resistance 3d info inductors for integrated voltage regulator applications," in *2016 IEEE International Electron Devices Meeting (IEDM)*, 2016, pp. 35.2.1–35.2.4.

[38] K. Tien *et al.*, "An 82with on-chip magnetic inductors," in *2015 Symposium on VLSI Circuits (VLSI Circuits)*, 2015, pp. C192–C193.

[39] J. T. DiBene *et al.*, *A 400 amp fully integrated silicon voltage regulator with in-die magnetically coupled embedded inductors*, APEC - Special Presentation, 2010.

[40] N. Wang *et al.*, "Integrated magnetics on silicon for power supply in package (psip) and power supply on chip (pwrsoc)," in *3rd Electronics System Integration Technology Conference ESTC*, 2010, pp. 1–6.

[41] G. Schrom *et al.*, "A 100mhz eight-phase buck converter delivering 12a in 25mm2 using air-core inductors," in *APEC 07 - Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition*, 2007, pp. 727–730.

[42] Altera, *En5322qi 2a powersoc synchronous buck dc-dc converter with integrated inductor*, 2018.

[43] E. Corporation, *Drgan plus development board epc9201/3 quick start guide*.

[44] Microchip, *Mic28303 50v 3a power module*, 2017.

[45] A. Barner, J. Wittmann, T. Rosahl, and B. Wicht, "A 10 mhz, 48-to-5v synchronous converter with dead time enabled 125 ps resolution zero-voltage switching," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 106–110.

[46] M. Chen, P. S. Shenoy, and J. Morroni, "A series-capacitor tapped buck (sc-tab) converter for regulated high voltage conversion ratio dc-dc applications," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 3650–3657.

[47] J. Wittmann, T. Funk, T. Rosahl, and B. Wicht, "A 48-v wide- V_{in} 9–25-mhz resonant dc–dc converter," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 7, pp. 1936–1944, 2018.

[48] T. Instruments, *Using the lmg5200polevm-10 48v to point of load evm*, 2016.

[49] S. S. Kudva and R. Harjani, "Fully-integrated on-chip dc-dc converter with a 450x output range," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 8, pp. 1940–1951, 2011.

[50] C. Huang and P. K. T. Mok, "An 84.7integrated buck converter with precise dcm operation and enhanced light-load efficiency," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 11, pp. 2595–2607, 2013.

[51] K. Bharath and S. Venkataraman, "Power delivery design and analysis of 14nm multicore server cpus with integrated voltage regulators," in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, 2016, pp. 368–373.

[52] M. Gong, X. Zhang, and A. Raychowdhury, "Non-isolated 48v-to-1v heterogeneous integrated voltage converters for high performance computing in data centers," in *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2020, pp. 411–414.

[53] A. Lidow, J. Strydom, M. de Rooij, and D. Reusch, 2nd ed. John Wiley and Sons Ltd., 2015, ISBN: 978-1-118-84476-2.

[54] M. L. F. Bellaredj, S. Mueller, A. K. Davis, P. Kohl, M. Swaminathan, and Y. Mano, "Fabrication, characterization and comparison of fr4-compatible composite magnetic materials for high efficiency integrated voltage regulators with embedded magnetic core micro-inductors," in *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*, 2017, pp. 2008–2014.

[55] T. Guillod, P. Papamanolis, and J. W. Kolar, "Artificial neural network (ann) based fast and accurate inductor modeling and design," *IEEE Open Journal of Power Electronics*, vol. 1, pp. 284–299, 2020.

[56] H. M. Torun and M. Swaminathan, "High-dimensional global optimization method for high-frequency electronic design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 6, pp. 2128–2142, 2019.

[57] Y. Yang, S. Zeng, H. Long, Z. Yan, D. Yu, and L. Kang, "Automated wire antennas design using dynamic dominance evolutionary algorithm," in *2009 NASA/ESA Conference on Adaptive Hardware and Systems*, 2009, pp. 257–262.

[58] K. Qin, S. Zeng, Z. Li, and H. Jing, "Automated antenna design using self-adaptive differential evolution algorithm," in *2011 Fourth International Conference on Intelligent Computation Technology and Automation*, vol. 2, 2011, pp. 964–969.

[59] A. Pichler, D. Steffelbauer, and A. Nazarov, "Examples for genetic algorithm based optimal rfid tag antenna design," in *2014 IEEE RFID Technology and Applications Conference (RFID-TA)*, 2014, pp. 223–227.

[60] P. Raj *et al.*, *Novel nanostructured passives for rf and power applications: Nanopackaging with passive components*, 2015.

[61] M. L. F. Bellaredj, S. Mueller, A. K. Davis, Y. Mano, P. A. Kohl, and M. Swaminathan, "Fabrication, characterization and comparison of composite magnetic materials for high efficiency integrated voltage regulators with embedded magnetic core micro-inductors," *Journal of Physics D: Applied Physics*, vol. 50, no. 45, p. 455 001, 2017.

[62] H. Song, *Soft magnetic composites for high frequency applications*, 2015.

[63] Tokin Kemet Company, *Soft magnetic metal-flake composite material suitable for high frequency power modules*, 2019.

[64] G. Bertotti, "Chapter 3 - maxwell's equations in magnetic media," in *Hysteresis in Magnetism*, ser. Electromagnetism, G. Bertotti, Ed., San Diego: Academic Press, 1998, pp. 73 –102, ISBN: 978-0-12-093270-2.

[65] R. Ramprasad, P. Zurcher, M. Petras, M. Miller, and P. Renaud, "Magnetic properties of metallic ferromagnetic nanoparticle composites," *Journal of Applied Physics*, vol. 96, no. 1, pp. 519–529, 2004.

[66] B. M. Moskowitz, *Hitchhiker's guide to magnetism*, 1991.

[67] M. L. Ababsa, O. Ninet, G. Velu, and J. P. Lecointe, "High-temperature magnetic characterization using an adapted epstein frame," *IEEE Transactions on Magnetics*, vol. 54, no. 6, pp. 1–6, 2018.

[68] N. Takahashi, M. Morishita, D. Miyagi, and M. Nakano, "Examination of magnetic properties of magnetic materials at high temperature using a ring specimen," *IEEE Transactions on Magnetics*, vol. 46, no. 2, pp. 548–551, 2010.

[69] S. L. Selvaraj *et al.*, "On-chip thin film inductor for high frequency dc-dc power conversion applications," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 176–180.

VITA

Claudio Alvarez Barros was born in 1984 in Santiago, Chile. He received the B.S. degree in electrical engineering from the Universidad de Santiago de Chile, in 2009. From 2010 to 2012, he worked in the international ALMA Radio Observatory. After that, he worked in other companies as an electronic and robotic engineer. In 2016 he was granted with a Fulbright fellowship from the US government and a CONICYT scholarship from the government of Chile to pursue a Ph.D. degree in the United States. In 2017 he started the Electrical and Computer Engineering Ph.D. program in the Georgia Institute of Technology. In May of 2019 he received the M.S. degree and in July of 2021 he received Ph.D.